SEMICONDUCTOR DATA BOOK

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CONTENTS

GENERAL INFORMATION

As the present condition, demand the various needs, the computer system will be strongly required more high-speed functions. Hitachi provide the two types of the standard high-speed logic IC which keep the high market share, the Schottky TTL and the ECL of unsaturated type. The Schottky TTLs are practically provided same circuits configuration and operating characteristics as the standard TTL. In the case of the saturated type logic IC, during the transistor turn on, among the B-to-E and B-to-C of the front junction is holdering the forward bias, and the carrier charge is stored in the bias area.

When the transistor turn off, the stored charge must be discharged electricity through the connector, so that the time to take extinction of charge is caused putting back the transistor. This stored delay time is common with all saturated type logic IC. The Schottky TTLs reduce the delay time that B-to-C junction clamped by the Schottky diode and controled the forward bias between B and E. The Schottky diodes surely control the saturation in transistors, in the other hand increasing the input capacity in clamped transistor, the operating speed becomes faster than TTL, but it meets limits to improve for RC-time constant in the transistor's input circuits.

The ECL which has designed by unsaturated technology dose not have the stored delay time, improvement for operating speed does not meet the limits.

The ECLs are running on the top of high speed logic ICs as semiconductor devices, moreover this technology has enough furture.

Hitachi developped HD10K series (compatible with Motorola 10K series), and HD100K series (compatible with Fairchiled F100K series) which operate at a high speed (three times faster than HD10K series), and which immune from the influence by temperature and power variation. HD100K series are the newest semiconductor devices realized the above switching speed, employ the 3μm fine pattern process and the ion implantation, realized the reduction of cell size and the improvement of frequency characteristics.

Fig. 1 and Table 1 show the functional index in gates of the typical digital ICs.

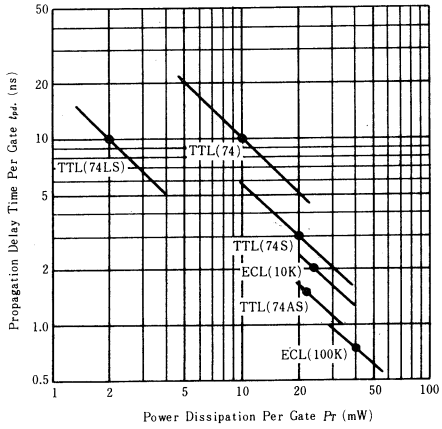


Fig.1 Propagation Delay Time vs. Power Dissipation

Table 1. Comparison of the Speed-Power Product

	HD100K	HD10K	HD74	HD74S	HD74LS
Propagation Delay Time	0.75ns	2ns	10ns	3ns	10ns
Power Dissipation	40mW	25mW	10mW	20mW	2mW
Speed-Power Product	30pJ	50pJ	100pJ	60pJ	20pJ

DEFINITIONS OF LETER SYMBOLS AND ABBREVIATIONS

Symbol	Abbreviations
I_{EE}	Total power supply current drawn from a ECL test unit by the negative power supply
I_{CC}	Total power supply current drawn from the positive supply by a ECL unit under test
I_F	Forward diode current drawn from an input of a TTL-to-ECL translator when that input is at ground potential
I_{IH}	High level input current, into a node with a specified High level (V_{IH} max) logic voltage applied to that node
I_{IL}	Low voltage input current, into a node with a specified Low level (V_{IL} min) logic voltage applied to that node
I_{OH}	High level output current: the current flowing into the output, at a specified High level output voltage
I_{OL}	Low level output current: the current flowing into the output, at a specified Low level output voltage
I_{out}	Output current (from a device or circuit, under such conditions mentioned in context)
I_R	Reverse current drawn from a transistor input of a test unit when V_{EE} is applied at that input
I_{SC}	Short-circuit current drawn from a translator saturating output when that output is at ground potential
V_{BB}	Reference bias supply voltage
V_{CC1} (V_{CC})	Most positive power supply voltage (output devices)
V_{CC2} (V_{CCA})	Most positive power supply voltage (current switches and bias driver)
V_{EE}	Most negative power supply voltage for a circuit
V_{TT}	Line load-resistor terminating voltage for outputs from a ECL device
V_{in}	Input voltage (to a circuit or device)
V_{out}	Output voltage
V_{max}	Maximum (most positive) supply voltage, permitted under a specified set of conditions
V_{IH} max	Maximum High level input voltage: The most positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed
V_{IHA} min (V_{IH} min)	Minimum input logic High level (threshold) voltage for which performance is specified
V_{ILA} max (V_{IL} max)	Maximum input logic Low level (threshold) voltage for which performance is specified
V_{IL} min	Minimum Low level input voltage: The least positive (most negative) value of Low level input voltage for which operation of the logic element within specification limits is guaranteed
V_{OH} max	Maximum output High or high-level voltage for given inputs
V_{OH} min	Minimum output High or high-level voltage for given inputs
V_{OHA} (V_{OHC})	Output logic High threshold voltage level
V_{OLA} (V_{OLC})	Output logic Low threshold voltage level
V_{OL} max	Maximum output Low level voltage for given inputs
V_{OL} min	Minimum output Low level voltage for given inputs
t_{TLH}	Wave form rise time (Low to High)
t_{THL}	Wave form fall time (High to Low)
t_{PLH}, t_{PHL}	Propagation delay time, 50% to 50%
t_{su}	Set-up time of a flip-flop or counter device
t_h	Hold time of a flip-flop or counter device
f_{Tog}	Toggle frequency of a flip-flop or counter device

( ) : apply to the HD100K series only

GENERAL INFORMATION OF HD10K SERIES

■FEATURES

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters. High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

Low Cross-Talk due to low-current switching in signal path and small (typically 850mV) voltage swing, and to relatively long rise and fall times.

Transmission Line Drive Capability is afforded by the open emitter outputs of ECL devices. No "Line Drivers" are listed in ECL families, because every device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

■BASIC CONSIDERATIONS FOR HIGH-SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.
2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.
3. The possibility of "crosstalk" between adjacent signal leads is proportionately increased in high-speed systems.
4. Electrical noise generation and pick-up are more detrimental at higher speeds. In general, these four characteristics are speed-and frequency-dependent, and are virtually independent of the type of logic employed.

The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nano-seconds, an equivalent "gate delay" is introduced for every foot of interconnecting wiring.

Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant.

But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. ECL circuits, particularly those of the ECL 10K Series are designed with a propensity toward complex functions to enhance overall system speed.

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem.

At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 2). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run.

The low-impedance, emitter-follower outputs of ECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.

The increased affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal.

These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. In the design of ECL 10K, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.

From the above, it is evident that the ECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.

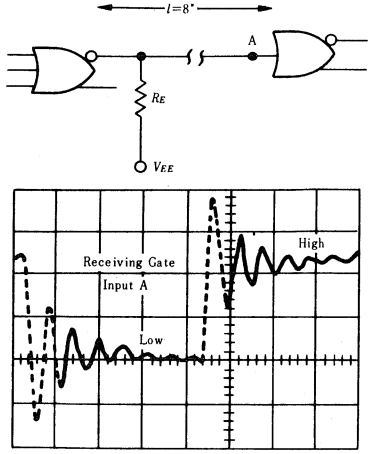


Fig.2a Unterminated Transmission Line (No Ground Plane Used)

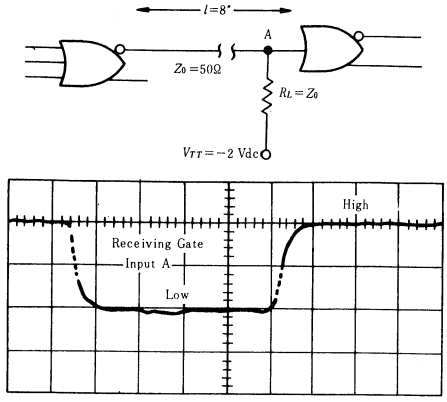


Fig.2b Properly Terminated Transmission Line (Ground Plane Added)

CIRCUIT DESCRIPTION

The typical ECL circuit, Figure 3, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function.

Power-Supply Connections — Any of the power supply levels V_{TT}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case; V_{CC}=0, V_{TT}=−2.0V, V_{EE}=−5.2V.

System Logic Specifications — The output logic swing of 0.85V, as shown by the typical transfer characteristics curve, varies from a LOW state of V_{OL}=−1.75V to a HIGH state of V_{OH}=−0.9V with respect to ground.

Positive logic is used when reference is made to logical "0"s or "1"s Then

"0" = -1.75V = LOW
"1" = -0.9V = HIGH typical

Circuit Operation — Beginning with all logic inputs LOW (nominal −1.75V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting.

Under these conditions, with the base of Q5 heid at −1.29V by the V_{BB} network, its emitter will be one diode drop (0.8V) more negative than its base, or −2.09V. (the 0.8V differential is a characteristic of this P-N junction.)

The base-to-emitter differential across Q1 — Q4 is then the difference between the common emitter voltage (−2.09V) and the LOW logic level (−1.75V) or 0.34V.

This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off. When any one (or all) of the logic inputs are shifted upward from the −1.75V LOW state to the −0.9V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on.

When this happens, the voltage at the common-emitter point rises from −2.09V to −1.7V (one diode drop below the −0.9V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at −1.29V, the base-emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off. This action is reversible, so that when the input signal(s) return to the LOW state, Q1 — Q4 are again turned off and Q5 again becomes forward biased.

The collector voltages resulting from the switching action of Q1 — Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

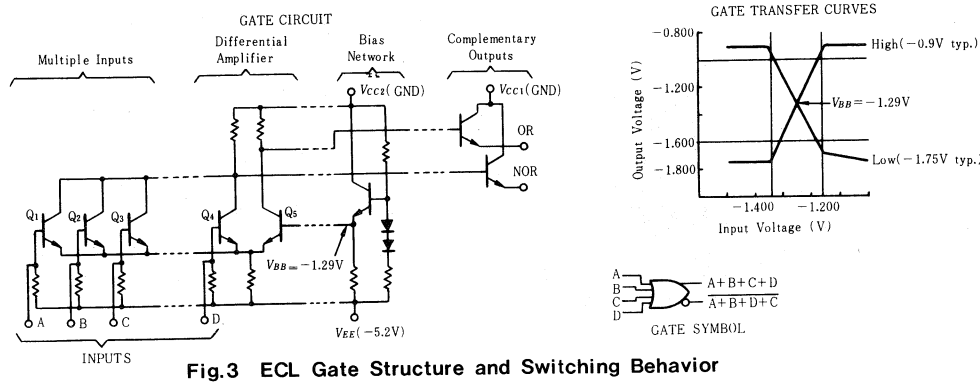


Fig.3 ECL Gate Structure and Switching Behavior

■TECHNICAL DATA

In subsequent sections of this Data Book, the important ECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section. In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits; Transfer Characteristics, which define logic levels and switching thresholds; DC Parameters, such as output levels, threshold levels, and forcing functions. AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with ECL circuits.

●Maximum Ratings

Table 1

Item	Symbol	Rating	Unit
Supply Voltage*	V_{EE}	−8~0	V
Input Voltage*	V_{in}	0~V_{EE}	V
Output Current	I_O	50	mA
Surge Output Current	$I_{O(surge)}$	100	mA
Junction Temperature	T_j	125	°C
Storage Temperature	T_{stg}	−55~+125	°C

* Value at V_{CC}=GND

●Recommended Operating Conditions

Table 2

Item	Symbol	Value	Unit
Operating Temperature Range	T_A	−30 to +85	°C
D.C. Fan Out		70	
Supply Voltage Range	V_{EE}	−5.2±10%	V

●Transfer Curves

For ECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. A typical transfer curve and associated data for all ECL families is shown in Figure 4.

It is not necessary to measure transfer curves at all points of the curves.

To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

The first set is obtained by applying test voltages, V_{IL} min and V_{IH} max (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between V_{OL} max and V_{OL} min, and V_{OH} max and V_{OH} min specifications.

The second set of logic level parameters relates to the switching thresholds.

This set of data is distinguished by an "A" in symbol subscripts.

A test voltage, V_{ILA} max, is applied to the gate and the NOR and OR outputs are measured to see that, they are above the V_{OHA} min and below the V_{OLA} max levels, respectively. Similar checks are made using the test input voltage V_{IHA} min. The result of these specifications insures that:

a) The switching threshold ($-V_{BB}$) falls within the darkest rectangle; i.e. switching does not begin outside this rectagle;

b) Quiescent logic levels fall in the lightest shaded ranges;

Table 3 shows the guaranteed ECL 10K series logic levels and switching thresholds.

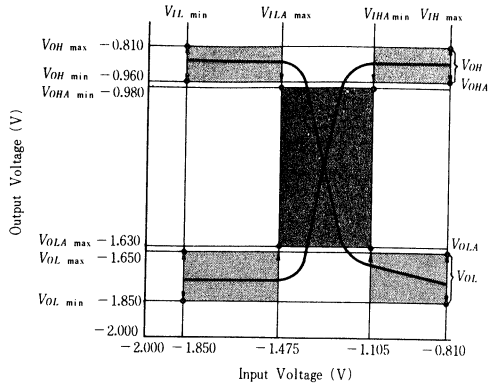


Fig.4 Transfer Curves(HD10K Example)

Figure 5 shows the typical transfer characteristics as a function of temperature.

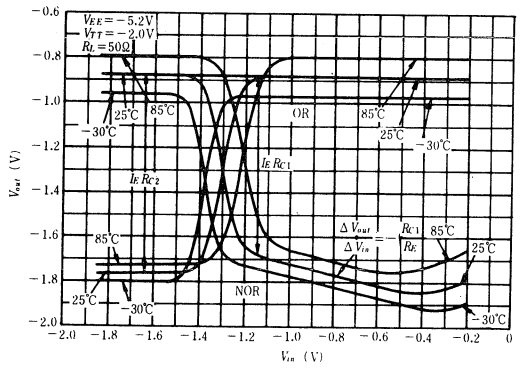


Fig.5 The Transfer Curves for Temperature Variations.

Table 3 D.C Specification Test Points (HD10K Example)

Input	Output	Value	Unit
V_{IL} min		−1.850	V
V_{IH} max		−0.810	
	V_{OL} min	−1.850	
	V_{OL} max	−1.650	
	V_{OH} min	−0.960	
	V_{OH} max	−0.810	
V_{ILA} max		−1.475	
V_{IHA} min		−1.105	
	V_{OLA} max	−1.630	
	V_{OHA} min	−0.980	
With suitable inputs :			
Typical Output HIGH State		−0.900	
Typical Output LOW State		−1.750	
Nominal V_{BB}(Switching Threshold)		−1.290	

Test Conditions;

V_{EE} = -5.2V, V_{CC} = 0V, Ta = 25°C,

after thermal equilibrium has been established on airflow greater than 500 linear fpm is maintained.

Outputs loaded 50Ω to −2.0Vdc

Table 4 The Temperature Coefficients

		Ta=−30~+25°C	Ta=+25~+85°C
"1" Level	$\Delta V_{IHA}/\Delta T$	1.82mV/°C	1.16mV/°C
	ΔV_{OHA} min/ΔT	1.82mV/°C	1.16mV/°C
	$\Delta V_{NH}/\Delta T$	1.82mV/°C	1.16mV/°C
"0" Level	$\Delta V_{ILA}/\Delta T$	0.46mV/°C	0.58mV/°C
	ΔV_{OLA} max/ΔT	0.46mV/°C	0.58mV/°C
	$\Delta V_{NL}/\Delta T$	0.46mV/°C	0.58mV/°C

Table 4 show the temperature coefficiemts of ECL IOK DC parameters.

Figure 6 shows the transfer characteristic data obtained for a variety of supply voltages.

Table 5 indicates the change rates of output voltages as a function of power supply voltages.

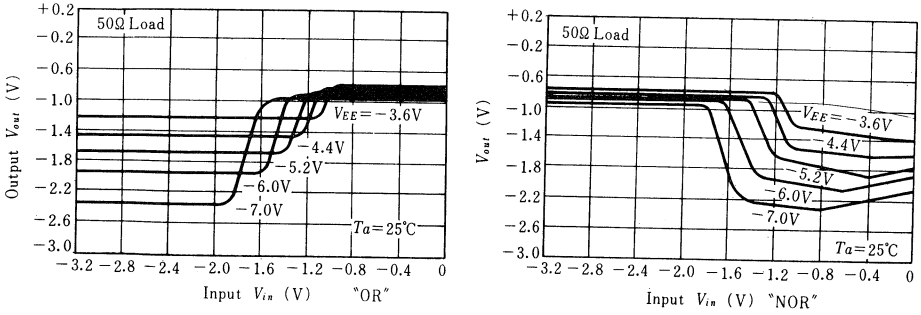


Fig.6 The Transfer Curves for power supply variations

Table 5 Typical Level Change Rates

$\Delta V_{OH}/\Delta V_{EE}$	0.016
$\Delta V_{OL}/\Delta V_{EE}$	0.250
$\Delta V_{BB}/\Delta V_{EE}$	0.148

● **Noise Margin**

"Noise margin" is a measure of a logic circuit's resistance to undesired switching. ECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript (V_{OHA} min, V_{OLA} max, V_{IHA} min, V_{ILA} max) in the transfer characteristic curves.

Guaranteed noise margin (NM) is defined as follows:

$NM_{HIGH\ LEVEL} = V_{OHA}$ min $- V_{IHA}$ min

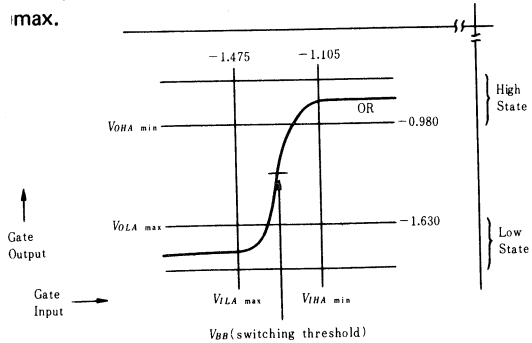
$NM_{LOW\ LEVEL} = V_{ILA}$ max $- V_{OLA}$ max

To see how noise margin is computed, assume a ECL gate drives a similar ECL gate, Figure 7. At a gate input (point B) equal to V_{ILA} max, ECL gate #2 can begin to enter the shaded transition region. This is a "worst case" condition, since the V_{OLA} max specification point guarantees that no device can enter the transition region before an input equal to V_{ILA} max is reached. Clearly then, V_{ILA} max is one critical point for noise margin computation, since it is the edge of the transition region.

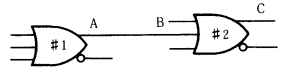
To find the other critical voltage, consider the output from ECL gate #1 (point A).

What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 7, it can be observed that the V_{OLA} max specification insures that the LOW state OR output from gate #1 can be no greater than V_{OLA} max. Note that V_{OLA} max is more negative than V_{ILA} max.

Thus, with V_{OLA} max at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of V_{ILA} max on the transfer curve.) In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from V_{OLA} max to V_{ILA} max.



Specification Points for Determining Noise Margin



This constitutes the "safety factor" known as noise margin.

It can be calculated as the magnitude of the difference between the two specification voltages, or for the ECL 10K levels shown:

$NM_{LOW} = V_{ILA}$ max $- V_{OLA}$ max = -1.475V − (-1.630V) = 155mV

Similarly, for the HIGH state:

$NM_{HIGH} = V_{OHA}$ min $- V_{IHA}$ min = -0.980V − (-1.105V) = 125mV

Analogous results are obtained when considering the "NOR" transfer data.

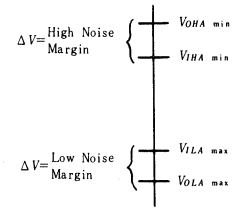
Note that these noise margins are absolute worst case conditions.

The lesser of the two noise margins is that for the HIGH state, 125mV.

This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances. As shown in the table, typical noise margins are usually better than guaranteed — by about 75mV.

Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on ECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise-margin specifications, but also other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state.

In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise-margin specifications.



Noise Margin Computations

Family	Guaranteed Worst-Case dc Noise Margin	Typical dc Noise Margin
ECL 10K	0.125	0.210

Fig.7 ECL Noise Margin Data

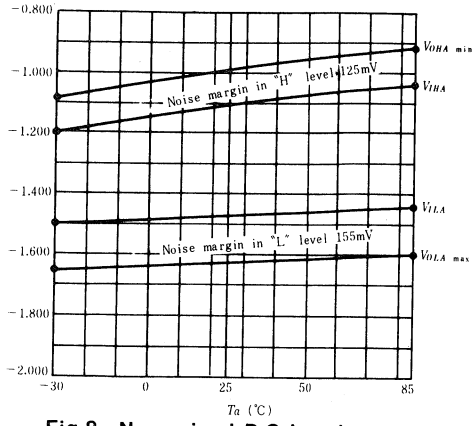


Fig.8 Normarized D.C Level vs. Temperature

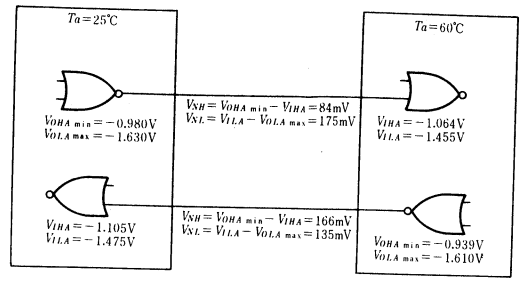


Fig.9 Noise margin in the case that has a difference of Temperature

● AC or Switching Parameters

Time-dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit.

They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, or access time, in the case of memories. Since this terminology has varied over the years, and because the "conditions" associated with a particular parameter may differ among logic families, the common ECL waveform and propagation delay terminologies are depicted in Figure 10.

Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for ECL 10K are given in the curves of Figure 11.

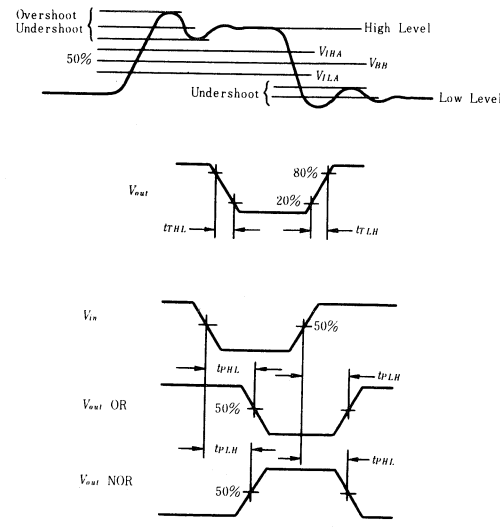


Fig.10 ECL Waveform and Propagation Delay

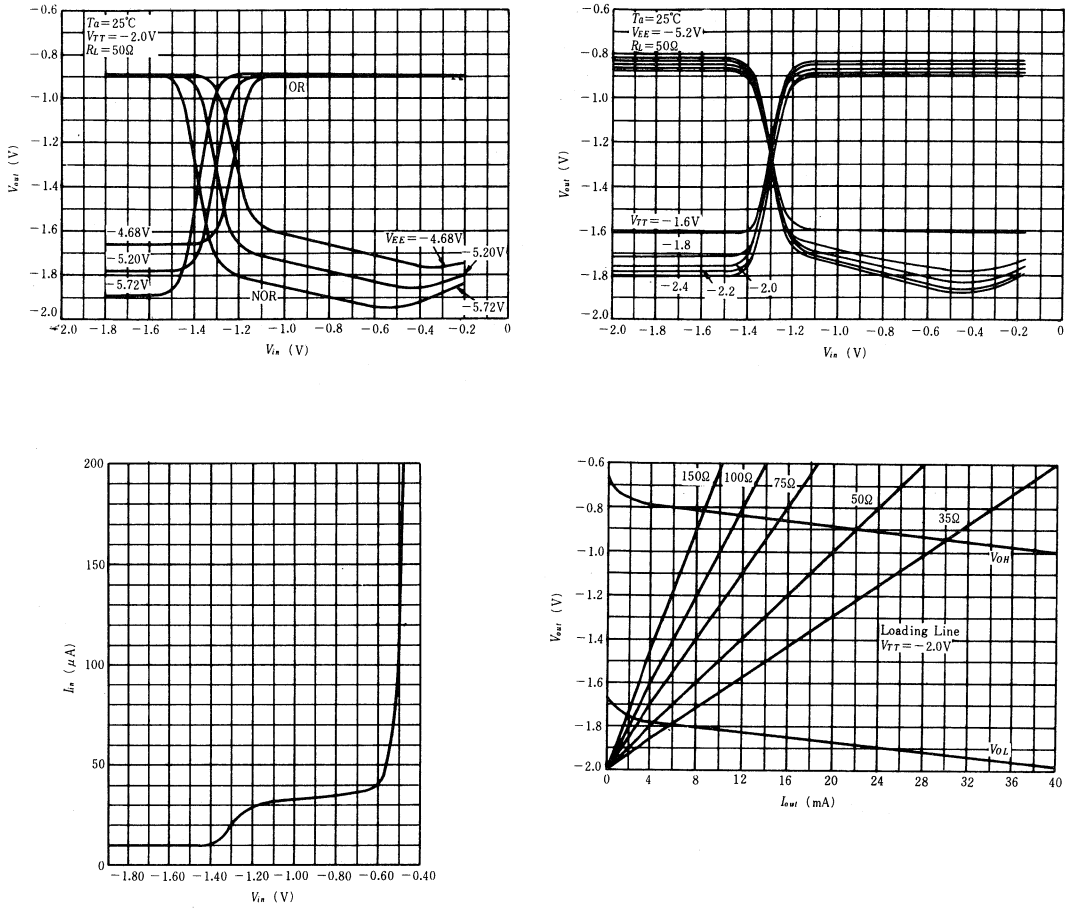


Fig.11 The characteristics of a Standard Gate

● Setup and Hold Times

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For ECL logic devices, t_{su} is the minimum time (50% – 50%) before the positive transition of the clock pulse (C) that information must be present at the Data input (D) to insure proper operation of the device.

The t_h is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 12.

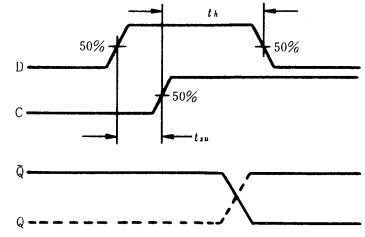
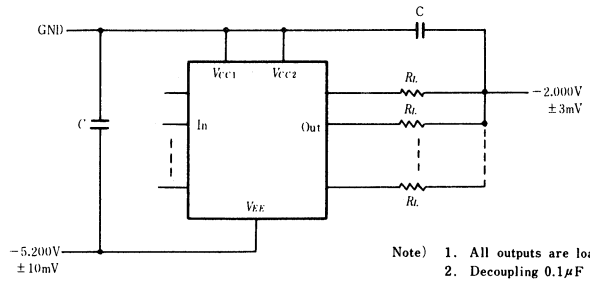


Fig.12 Setup and Hold Waveforms for ECL Logic Devices

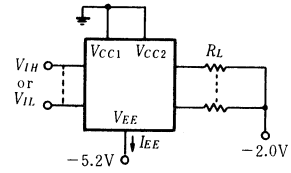
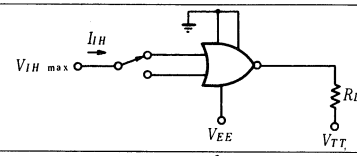
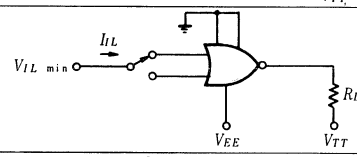
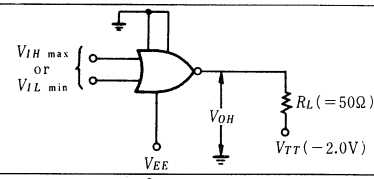
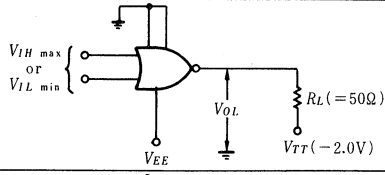
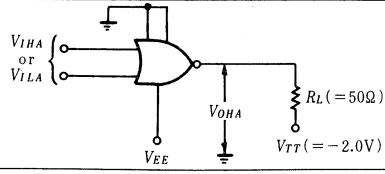
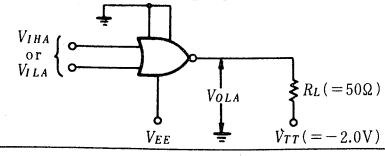
DIFFINITION OF SYMBOLS AND TESTING METHOD

DC Characteristics

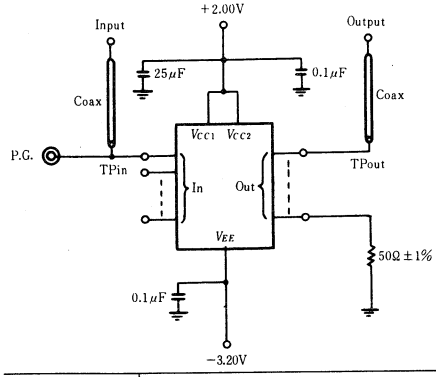


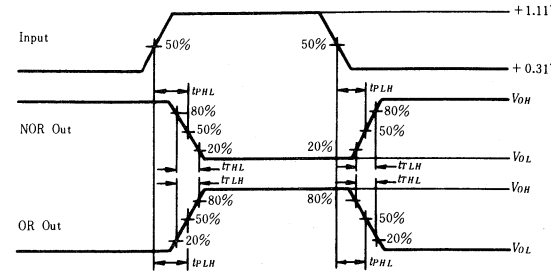
DC Characteristics

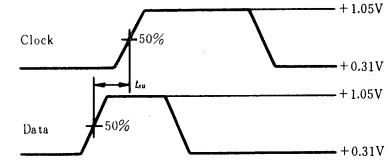
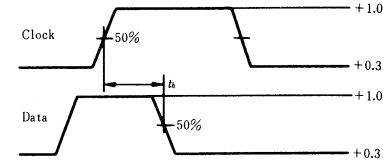
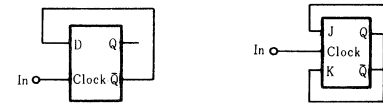
Note) 1. All outputs are loaded with 50Ω to GND (50Ω±1%)
2. Decoupling 0.1μF (25V) from GND to V_{CC} and V_{EE}
3. The tolerance of to shall be ±2℃

Item	Testing Method and Definitions
I_{EE}	The current required by each device from the V_{EE} supply 
I_{IH}	The current flowing into a device lead with specified V_{IH} applied to the input. 
I_{IL}	The current flowing into a device lead with specified V_{IL} applied to the input. 
V_{OH}	The voltage level at an output terminal with the specified output loading, with the specified conditions applied to establish a HIGH level at output. All outputs are loaded with 50Ω to V_{TT} (=-2.0V). 
V_{OL}	The voltage level at the output terminal with the specified output loading, with the specified conditions applied to establish a LOW level at the output. All outputs are loaded with 50Ω to V_{TT} (= −2.0V). 
V_{OHA}	The output HIGH threshold voltage with the inputs set to their respective threshold levels; V_{IHA} min or V_{ILA} max. 
V_{OLA}	The output LOW threshold voltage with the inputs set to their respective threshold levels; V_{ILA} max. or V_{IHA} min. 

●A.C Characteristics

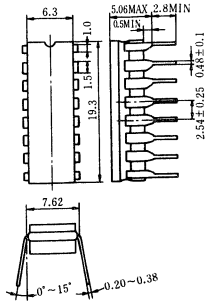




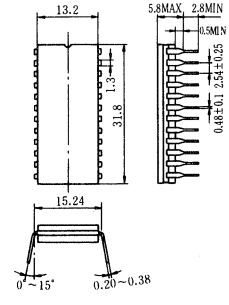
Item	Testing Method and Definitions
t_{TLH}	The time between two specified reference point (20%, 80%) on waveform which is changing from LOW to HIGH.
t_{THL}	The time between two specified reference point (20%, 80%) on waveform which is changing from HIGH to LOW.
t_{PLH} t_{PHL}	The time between the specified reference points on the input and output voltage waveforms with the output changing. (50% – 50% point)
t_{su}	The internal immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its recognition. 
t_h	The interval immediately following the active transition of the timing pulse or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at input to ensure its continued recognition. 
f_{Tog}	The maximum repetition rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device (flip-flop or counter) may cease to function. 

■PACKAGE(Unit : mm)

●16 Pin Ceramic Package



●24 Pin Ceramic Package



■OPTIONAL DATA

● Power Supply Considerations

ECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at −5.2V. While this ECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the ECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The −5.2V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect.

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by ECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0μF and a 100pF capacitor at the power entrance to the board, and a 0.01μF low-inductance capacitor between ground and the −5.2V line every four to six packages, are recommended.

Most ECL circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package when the outputs are driving heavy loads. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

● Power Dissipation

The power dissipation of ECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pull-down resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

The table in Figure 12 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor use; in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to −2.0 Vdc	5.0	4.3
100 ohms to −2.0 Vdc	7.5	6.5
75 ohms to −2.0 Vdc	10	8.7
50 ohms to −2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohms to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

Fig.12 Average Power Dissipation in Output Circuit with External Terminating Resistors.

The power dissipation of ECL functiinal blocks varies with both temperature and V_{EE}.

Typical variations are shown in Figure 13. The graph is normalized so that it applies to all ECL lines. The reference temperature is 25°C and the reference power is obtained by multiplying the typical I_E value (total power supply drain current specified on the data sheet) by V_{EE} (5.2V). For those devices where only the maximum value of I_E is specified on the data sheet, typical power dissipation is approximately 80% of that calculated with the I_E (max) specification.

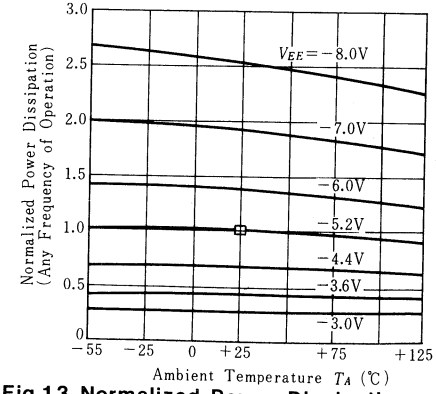


Fig.13 Normalized Power Dissipation vs. Temperature and Supply Voltage

● Loading Characteristics

The differential input to ECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with ECL circuits does not normally present a design problem. Graphs showing typical output voltage levels as a function of load current for ECL 10K are shown in Figure 14. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

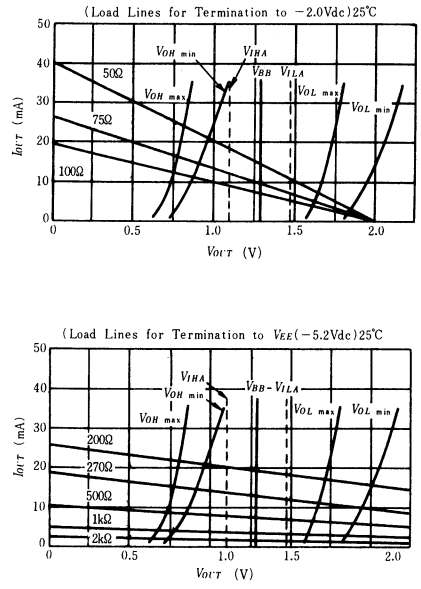


Fig.14 Output Voltage Levels vs. DC Loading

The affections of ac parameter by fanouts are shown in Figure 14-1.

Terminated transmission line signal interconnections are used for best ECL 10K system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are afected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1+Cd/Co}$.

Here Co is the normal intrinsic line capacitance, and Cd is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a ECL 10K transmission line vary with the line impedance. For example, with Zo=50 ohms, maximum stub length would be 4.5 inches. But when Zo=100 ohms, the maximum allowable stub length is decreased to 2.8 inches. The input loading capacitance of a ECL 10K gate is about 2.9pF.

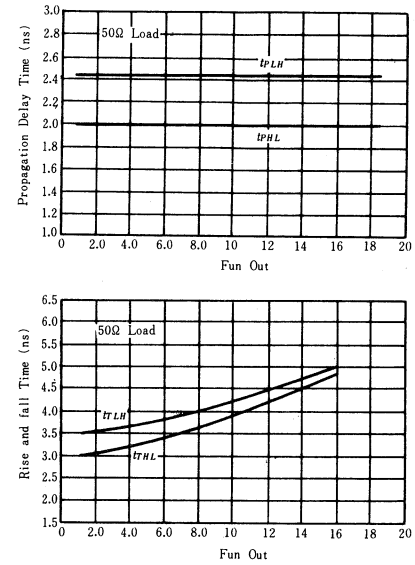


Fig.14-1 AC Parameter vs. Fanout

Therefore in order to keep the system speed, the recommended maximum fanout is defined within 10. (without to use the transmission line.)

● Unused ECL Inputs

All single-ended input ECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected. Input pulldown resistor values are typically 50 kohms and are not to be used as pulldown resistors for preceding open-emitter outputs.

Several ECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE}. (for example; HD10116)

■SYTEM DESIGN CONSIDERATIONS

● Thermal Management

Circuit performance and long-term circuit reliability are affected by die temperature.

Normally, both are improved by keeping the IC junction temperature low.

Electrical power dissipated in any integrated circuit is a source of heat.

This heat source increases the temperature of the die. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_j = T_A + P_D\ (\theta_{jc} + \theta_{CA})$$

or

$$T_j = T_A + P_D\ (\theta_{jA})$$

where

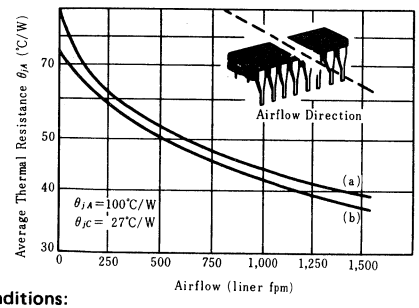
T_j = junction temperature
T_A = ambient temperature
P_D = power dissipation
θ_{jc} = average thermal resistance, junction to case
θ_{CA} = average thermal resistance, case to ambient
θ_{jA} = average thermal resistance, junction to ambient

Only two terms can be varied by the user-the ambient thermal resistance, θ_{CA}. Both system air flow and the package mounting technique affect the θ_{CA} thermal resistance term.

The maximum and average thermal resistance values for standard ECL IC package are given in Figure 15.

Package Type	θ_{jA}(°C/W)		θ_{jC}(°C/W)
	Maximum	Average	maximum
16 pin Ceramic Package	150	100	50
24 pin Ceramic Package	—	45	10

Fig.15 The Maximum and Average Thermal Resistance Values.



Conditions:
package; 16 pin Ceramic Package power dissipation; 200mW
measurement method; Diode Measurements
(a) Barnes socket
(b) PCB (10.2cm x 15.24cm x 1.6mm Cu)

Fig.16 Airflow vs. Thermal Resistance

The effect of air flow over the packages on θ_{jA} is illustrated in the graphs of Figure 16.

Fig. 17 shows the maximum power dissipation allowable at various ambient temperatures (still air) in a case of 16 pin ceramic dual in line package.

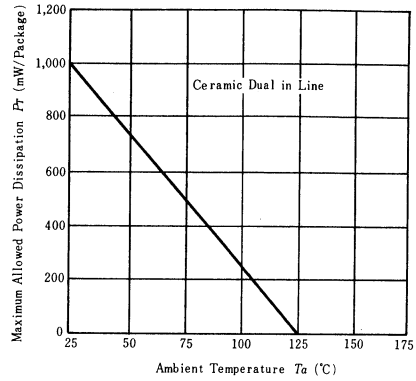


Fig.17 Ambient Temperature Derating Curve

● Interfacing ECL to Slower Logic Types

ECL circuits are interfaceable with MOS other logic forms. For ECL/TTL interfaces, when ECL is operated at the recommended −5.2 volts and TTL at +5V supply, currently available translator circuits, such as the HD10124 and HD10125, may be used.

For systems where a dual supply (−5.2V and +5V) is not practical, a discrete component translator can be designed. ECL also interfaces readily with MOS. With CMOS operating at +5V, any of the ECL to TTL translators works very well.

On the other hand, CMOS will drive ECL directly when using a common −5.2V supply.

● Circuit Interconnections

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high-speed logic cards.

Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages.

Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for ECL at top circuit speed, when high-density packaging is a requirement, or when transmission line interconnects are used. Point-to-point back-lane wiring without matched line terminations may be employed for ECL interconnections if line runs are kept short.

This applies to line runs up to 6 inches. But, because of the open-emitter outputs of ECL circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 18.

Resistor values for the connection in Figure 18a may range from 270 ohms to 2 kohms depending on power and load requirements. Power may be saved by connecting pull-down resistors in the range of 50 ohms to 150 ohms, to −2.0V dc, as shown in Figure 18b. Use of a series damping resistor, Figure 18c, will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length, while limiting overshood and undershoot to a predetermined amount.

Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance. The open emitter-follower outputs of ECL give the system designer all possible line driving options.

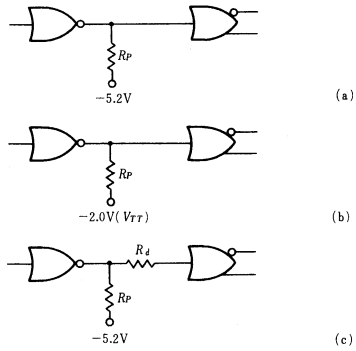


Fig.18 Pull-Down Resistor Techniques

One major advantage of ECL over saturated logic is its capability for driving matched-impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The ECL emitter-follower output transistors will drive a 50-ohm transmission line terminated to −2.0V dc. This is the equivalent current load of 22mA in the HIGH logic state and 6 mA in the LOW state.

Parallel termination of transmission lines can be done in two ways.

One, as shown in Figure 19a, uses a single resistor whose value is equal to the impedance (Zo) of the line. A terminating voltage (V_{TT}) of −2.0Vdc must be supplied to the terminating resistor. Another method of parallel termination uses a pair of resistors, R1 and R2, Figure 19b illustrates this method. The following two equations are used to calculate the values of R1 and R2:

R1 = 1.6Zo

R2 = R1·Z0/(R1-Z0)

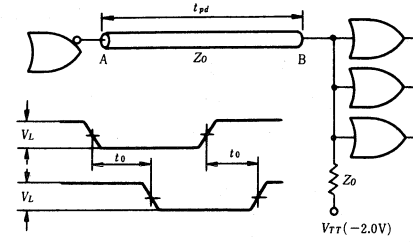


Fig.19-a Parallel Terminated Line

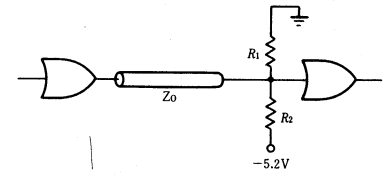


Fig.19-b Parallel Termination Thevenin Equivalent

Another popular approach is the series-terminated transmission line (see Figure 20).

This differs from parallel termination in that only one-half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

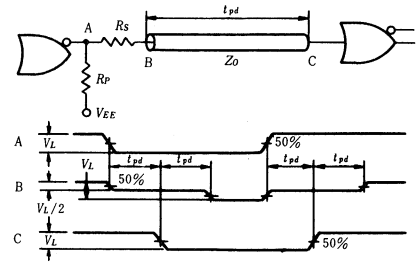


Fig.20 Series Terminated Line

To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by ECL circuits which have high impedance inputs. Using the appropriate terminating resistor (Rs) at point A (Figure 20), the reflections in the transmission line will be terminated. The advantages of series termination include ease of driving multiple series-terminated lines, low power consumption, and low cross talk

between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points. For board-to-board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies. No significant performance degradation occurs for lengths up to 50 feet for ECL.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any ECL function are connected to one end of the twisted pair line, and any ECL differential line receiver to the other as shown in the example, Figure 21. R_T is used to terminate the twisted pair line.

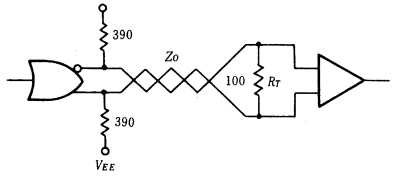


Fig.21 Twisted Pair Line Driver/Receiver

ECL signals may be sent very long distances (>1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made. If timing is critical, parallel signal paths (shown in Figure 22) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path. Wire-wrapped connections can be used with ECL. The mismatch occurs with ECL, but the distance between the wire-wrap connection and the end of the line is generally short enough so the reflections cause no problem.

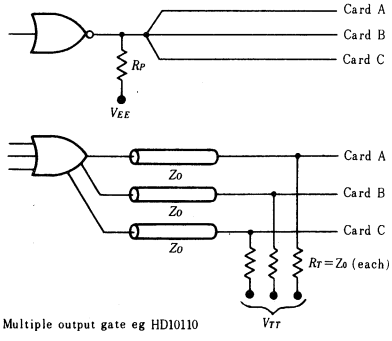


Fig.22 Parallel Fanout Techniques

Series damping resistors may be used with wire-wrapped lines to extend permissible backplane wiring lengths. The recommended wire-wrapped circuit cards have a ground plane on one side.

Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 23).

The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material. Stripline is used with multilayer circuit boards as shown in Figure 23. Stripline consists of a constant-width conductor between two ground planes.

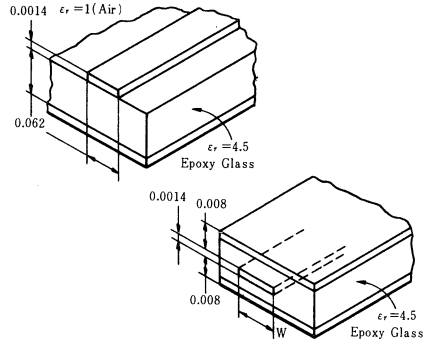


Fig.23 PC Interconnection Lines for use with ECL

● Clock Distribution

Clock distribution can be a system problem.

At ECL speeds, tither coaxial cable or twisted pair line can be used to distribute clock signals throughout a system.

Clock line lengths should be controlled and matched when timing could be critical.

Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of the application of this technique is shown in Figure 24.

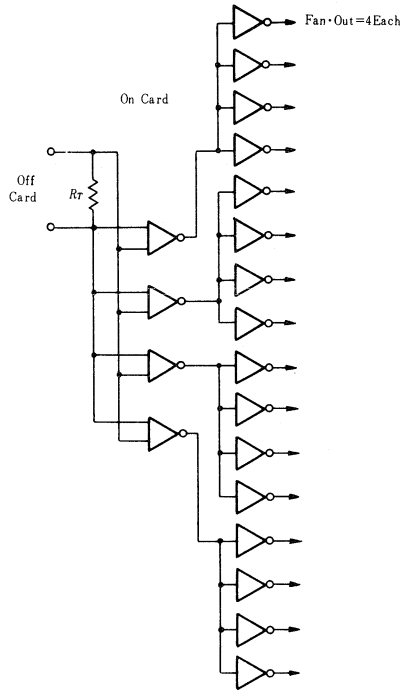


Fig.24 64 Fanout Clock Distribution

● **Logic Shortcuts**

ECL circuitry offers several logic design conveniences. Among these are:

1. Wire-OR (can be produced by wiring ECL output emitters together outside packages).
2. Complementary Logic Outputs (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 25.

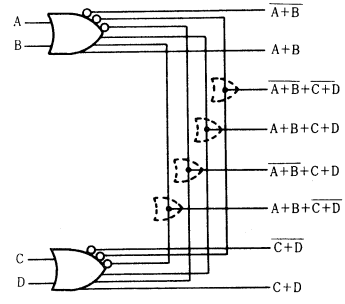


Fig.25 Example
(Use of Wire-OR and Complementary Outputs)

The connection shown saves four 2-input gates and two inverter over performing the same functions with saturated type logic.

Propagation delay is increased approximately 50 ps per wire-OR connection.

In general, wire-OR should be limited to 6 ECL outputs to maintain a proper LOW logic level. The use of a single output pulldown resistor is recommended per wire-OR, to economize on power dissipation.

● **Testing ECL Series**

To obtain results correlating with Hitachi circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 26. A solid ground plane is used in the test setup. All power leads and signal leads are kept as short as possible. The sampling scope interface runs directly to the 50-ohm inputs of Channel A and B via 50-ohm coaxial cable.

Equal-length coaxial cables must be used between the test set and the A and B scope inputs. The pulse generator must be capable of 2.0ns rise and fall times for ECL 10K. In addition, the generator voltage must have an offset to give ECL signal swings of ≈±400mV about a threshold of ≈+0.7V when V_{CC}=+2.0V and V_{EE}=−3.2V for ac testing of logic devices. The power supplies are shifted +2.0V, so that the device under test has only one resistor value to load into the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Hitachi and customer testing. Unused outputs are loaded with a 50-ohm resistor to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1μF, as is the V_{EE} pin.

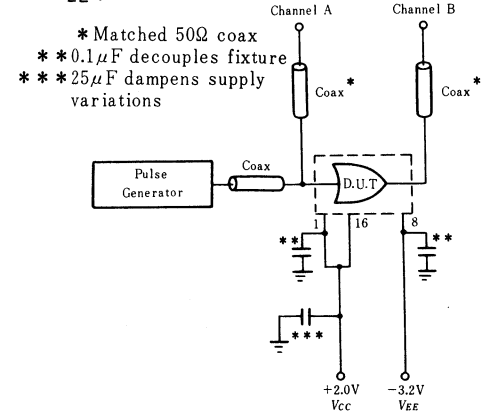


Fig.26 ECL Logic Switching Time Test Setup

GENERAL INFORMATION OF HD100K SERIES

■ FEATURES

● On-chip complementary output

Built-in complementary output requires no application of inverters, and it avoids the problems of number of external parts, power dissipation, propagation delay and so on.

● High input impedance and low output impedance

Due to the high input impedance (compared with TTL), more fan-out is obtained, and various circuit confideration is realized.

● Stability

Built-in temperature and voltage compensation circuits assure the stable output characteristics within all the temperature and the voltage ranges.

● Compatibility

HD100K series is fully compatible with F100K series on pin configulation, functions and characteristics.

■ ELECTRICAL CHARACTERISTICS ($Ta = 0 \sim +85℃$, $V_{EE} = -4.5V$, V_{CC} : GND)

Symbol	Item	min	typ	max	Unit	Conditions	
V_{OH}	Output Voltage High	−1025	−955	−880	mV	$V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$	$R_L = 50\Omega$ $V_{TT} = -2V$
V_{OL}	Output Voltage Low	−1810	−1705	−1620	mV		
V_{OHC}	Output Threshold Voltage High	−1035	—	—	mV	$V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$	
V_{OLC}	Output Threshold Voltage Low	—	—	−1610	mV		
V_{IH}	Input Voltage High	−1165	—	−880	mV		
V_{IL}	Input Voltage Low	−1810	—	−1475	mV		
I_{IL}	Input Current Low	0.5	—	—	μA	$V_{IN} = V_{IL\ min}$	

■ MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{EE}	−7.0	V
Input Voltage*	V_{in}	$0 \sim V_{EE}$	V
Output Current	I_O	50	mA
Surge Output Current	$I_{O(surge)}$	100	mA
Junction Temperature	T_j	150	℃
Storage Temperature	T_{stg}	−65～+150	℃

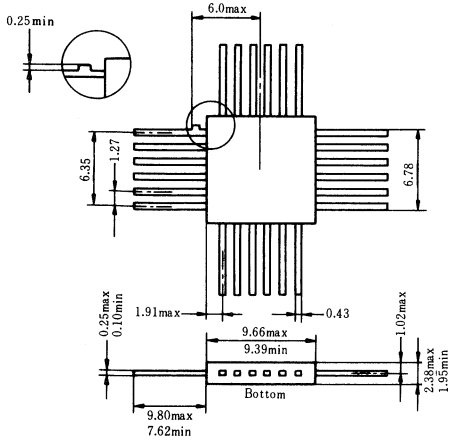
* Value at V_{CC} and V_{CCA} = GND

■ RECOMMENDED OPERATING CONDITIONS

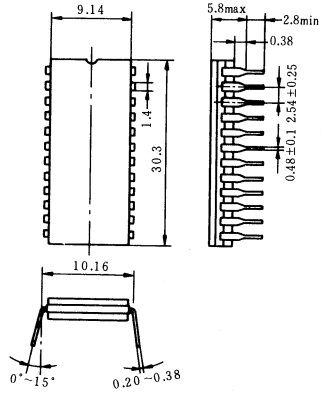
Item	Symbol	Value	Unit
Operating Temperature Range	T_A	0～85	℃
Supply Voltage Range	V_{EE}	−4.2～−5.7	V

■ PACKAGE

● 24 Pin Ceramic Flat Package (HD100KF Series)



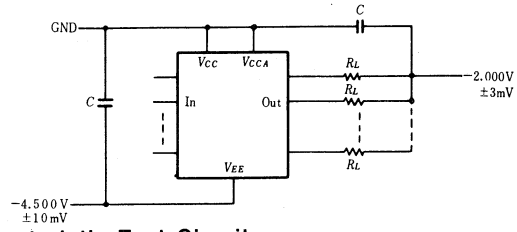
● 24 Pin Ceramic Dual-in-line Package (HD100K Series)



Package (Dimensions in mm)

■DEFINITION OF SYMBOLS AND TESTING METHOD

●DC Characteristics

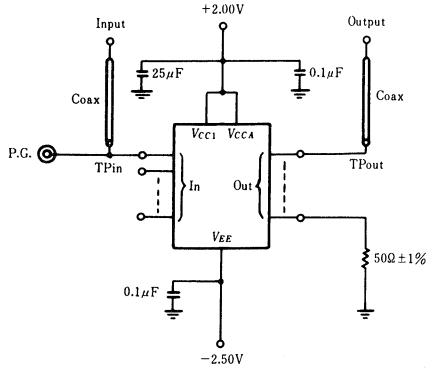


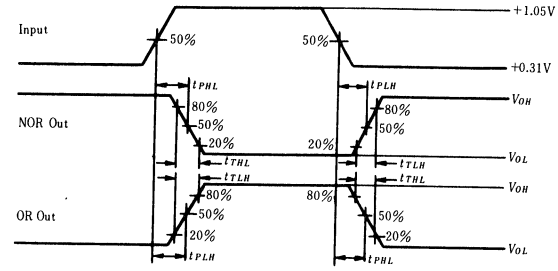
Note) 1. All outputs are loaded with 50Ω to GND (50Ω ± 1%)
2. Decoupling 0.1μF (25V) from GND to V_{CC} and V_{EE}
3. The tolerance of to shall be ± 2℃

●DC Characteristic Test Circuit

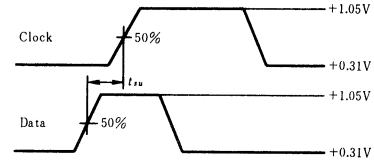
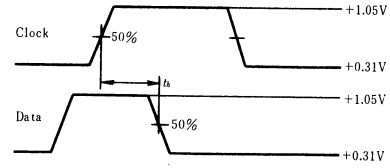
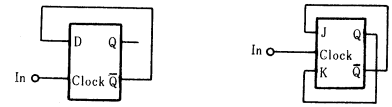
Item	Testing Method and Definitions
I_{EE}	The current required by each device from the V_{EE} supply.
I_{IH}	The current flowing into a device lead with specified V_{IH} applied to the input.
I_{IL}	The current flowing into a device lead with specified V_{IL} applied to the input.
V_{OH}	The voltage level at an output terminal with the specified output loading, with the specified conditions applied to establish a HIGH level at output. All outputs are loaded with 50Ω to V_{TT}(=−2.0V)
V_{OL}	The voltage level at the output terminal with the specified output loading, with the specified conditions applied to establish a LOW level at the output. All outputs are loaded with 50Ω to V_{TT}(=−2.0V)
V_{OHC}	The output HIGH threshold voltage with the inputs set to their respective threshold levels; V_{IH} min or V_{IL} max.
V_{OLC}	The output LOW threshold voltage with the inputs set to their respective threshold levels; V_{IL} max or V_{IH} min.

●AC Characteristics





Note) 1. Input pulse : $t_{TLH} = t_{THL} = 0.7 \pm 0.1$ns (20%~80%)
2. Unused outputs connected to a 50Ω resistoc to GND.
3. All input and output equal length 50Ω impedance lines R_T equal 50Ω termination of scope.
4. C_L=Jig stray capacitance≦ 3 pF.

Item	Testing Method and Definitions
t_{TLH}	The time between two specified reference point (20%, 80%) on waveform which is changing from LOW to HIGH.
t_{THL}	The time between two specified reference point (20%, 80%) on waveform which is changing from HIGH to LOW.
t_{PLH} t_{PHL}	The time between the specified reference points on the input and output voltage waveforms with the output changing. (50% – 50% point)
t_{su}	The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its recognition. 
t_h	The interval immediately following the active transition of the timing pulse or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at input to ensure its continued recognition. 
f_{Tog}	The maximum repetition rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device (flip-flop or counter) may cease to function. 

QUALITY ASSURANCE OF ECL

1. Views On Quality and Reliability

Basic views on quality in Hitachi are to meet individual users' purchase purpose and quality required, and to be at the satisfied quality level considering general marketability. Quality required by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize the quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance morale for quality. In addition, quality required by users on semiconductor devices are going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

(1) Build the reliability in design at the stage of new product development.
(2) Build the quality at the sources of manufacturing process.
(3) Execute harder the inspection and reliability confirmation of final products.
(4) Make quality level higher with field data feed back.
(5) Cooperate with research laboratories for higer quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. Reliability Design of Semiconductor Devices

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability tragets, timely sude and execution of design standardization, device design (include process design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishment of design rule, and standardization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc.

Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Site

Test site is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of Test Site are as follows
- Making clear about fundamental failure mode
- Analysis of relation between failure mode and manufacturing process condition
- Search for failure mechanism analysis
- Establishment of QC point in manufacturing

2. Effectiveness of evaluation by Test Site are as follows;
- Common fundamental failure mode and failure mechanism in devices can be evaluated.
- Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
- Able to analyze relation between failure causes and manufacturing factors.
- Easy to run tests.

etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competition

power of products, the major purpose of design review is to insure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows:

(1) Description of the products based on specified design documents.

(2) From the standpoint of speciality of individual participants, design documents are studied, and if unclear matter is found, sub program of calculation, experiments, investigation, etc. will be carried out.

(3) Determine contents of reliability and methods, etc. based on design document and drawing.

(4) Check process ability of manufacturing line to achieve design goal.

(5) Discussion about preparation for production.

(6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.

(7) Reference of past failure experiences with similar devices, confirmation of method to prevent them, and planning and execution of test program for confirmation of them. These study and decision are made using check lists made individually depending on the objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows:

(1) Problems in individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.

(2) Feedback of information should be made to insure satisfied level of process ability.

(3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability test.

3.2 Quality Approval

To insure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2. The views on quality approval are as follows;

(1) The third party executes approval objectively from the stand point of customers.

(2) Fully consider past failure experiences and information from field.

(3) Approval is needed for design change and work change.

(4) Intensive approval is executed on parts material and process.

(5) Study process ability and fluctuation factor, and set up control points at mass production.

Considering the views mentioned above, quality approval shown in Fig. 1 is executed.

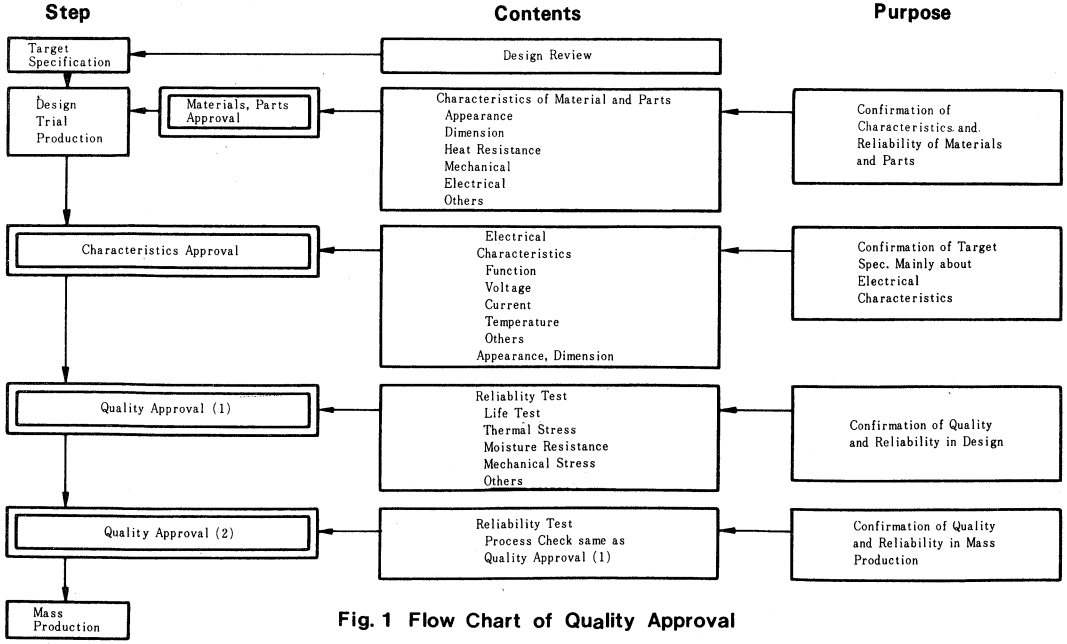


Fig. 1 Flow Chart of Quality Approval

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related.

The total function flow is shown in Fig. 2. The main points are described below.

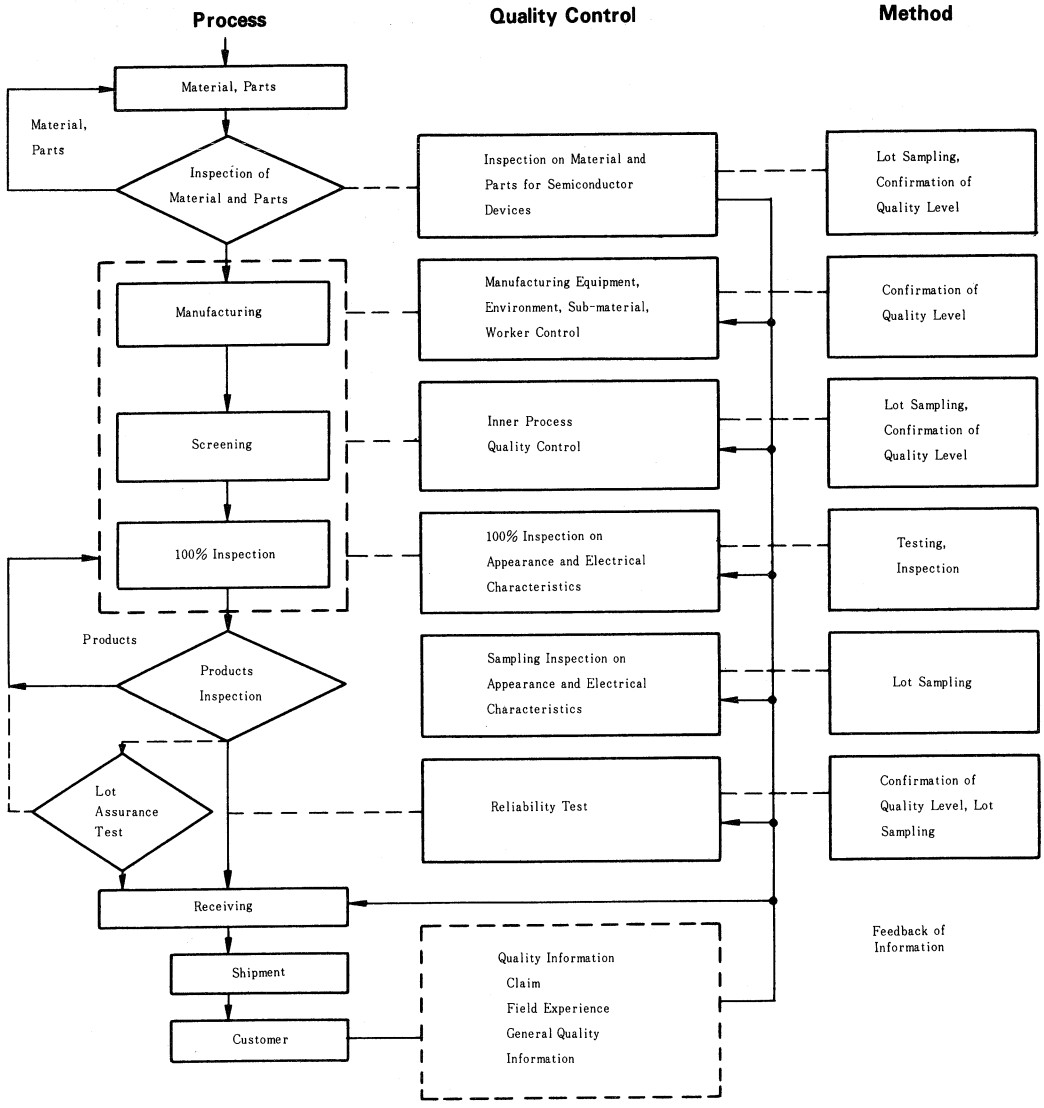


Fig. 2 Flow Chart of Quality Control in Manufacturing Process

3.3.1 Quality Control of Parts and Material

As tendency toward higher performance and higher reliability of semiconductor devices, is going, importance is increasing in quality control of material and parts, which are crystal lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials.

The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly. The other activities of quality assurance are as follows;

(1) Outside vendor technical information meeting

(2) Approval on outside vendors, and guidance of outside vendors

(3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

● **Table 1 Quality Control Check Points of Material and Parts (Example)**

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products manufacturing facilities, measuring equipments, circumstances and sub-materials. The manufacturing inner process quality control is shown in Fig. 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process.

Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and tighter inner process quality control is executed – rigid check in each process and each lot, 100% inspection pointed process to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semifinal products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of countermeasures
- Transfer of information about quality

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing equipments are extraordinary developing as higher performance devices are needed and improvement of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain prompt operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are checked one by one not to make any omission. As for adjustment and maintenance of measuring equipments, maintenance number, specification are

checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-materials

Quality and reliability of semiconductor device is highly affected by manufacturing process. Therefore, the controls of manufacturing circumstances—temperature, humidity, dust—and the control of submaterials—gas, pure water—used in manufacturing process are intensively executed. Dust control is described in more detail below. Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, air-conditioning systems, materials delivered-in, clothes, work, etc., and periodical inseption on floating dust in room, falling dusts and dirtiness of floor.

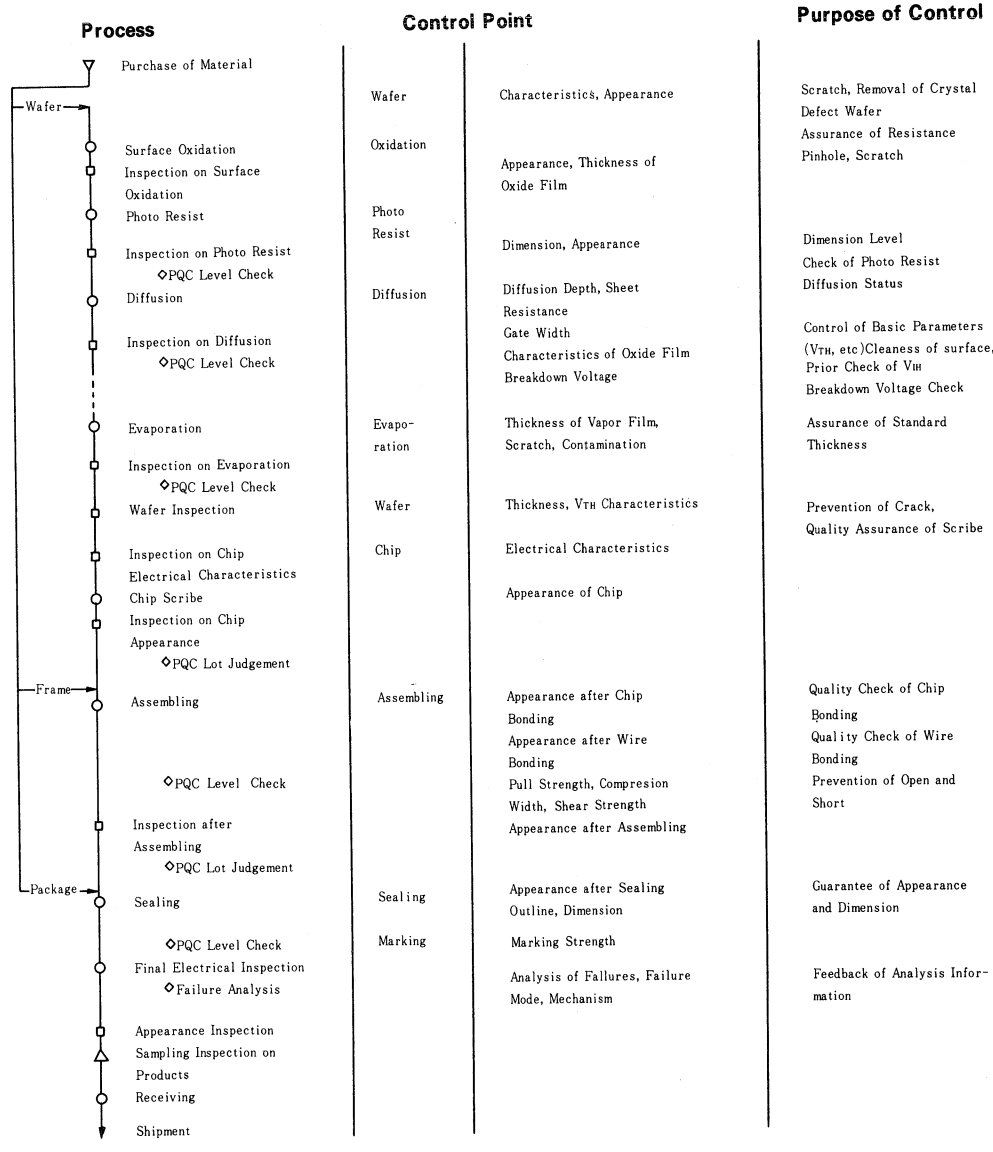


Fig. 3 Example of Inner Process Quality Control

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot insepction is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc..

The inspection is executed not only to confirm that the products meet users requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.

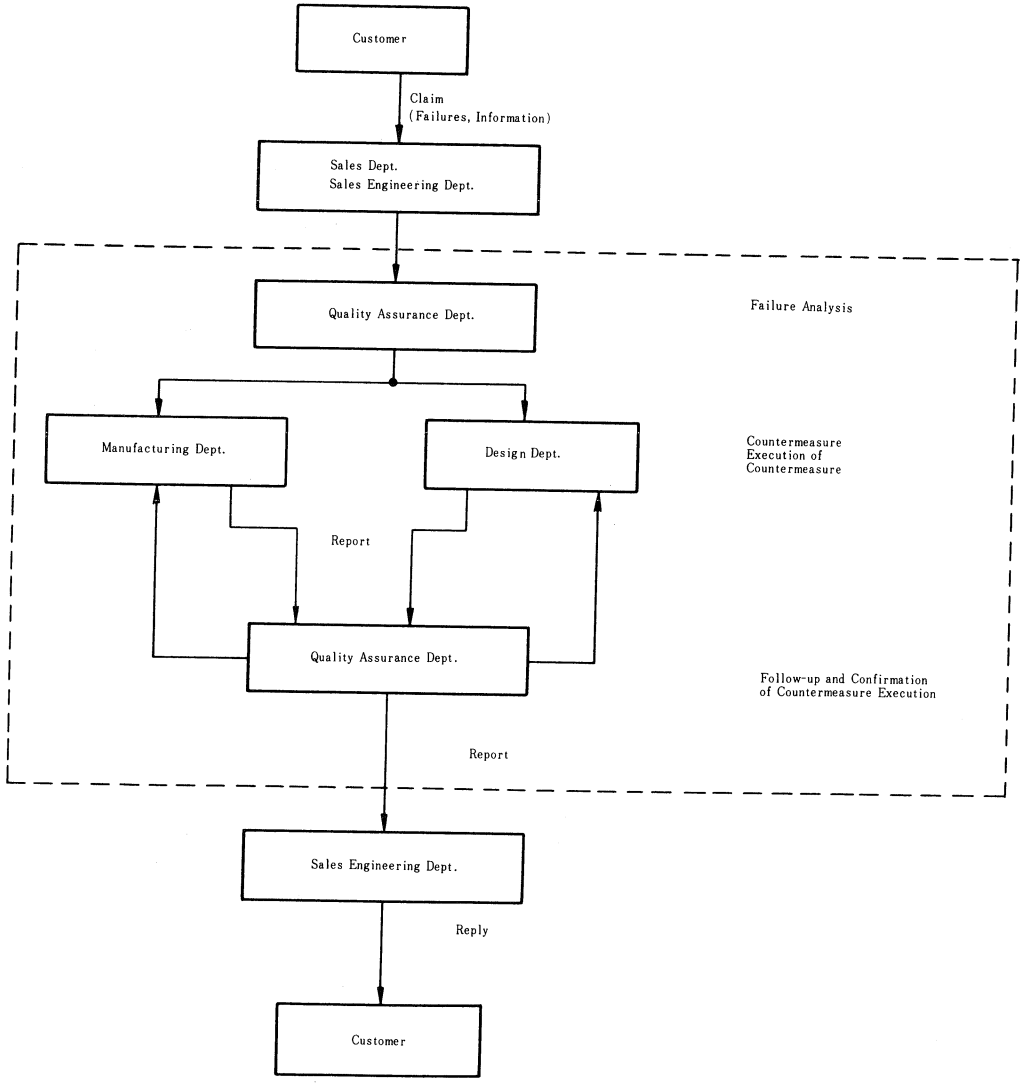


Fig. 4 Process Flow Chart of Field Failure

4. RELIABILITY OF ECL

4.1 Structure

ECL 10K features high integration and high speed due to greatly reduced logic stage number in circuit by vertical structure and collector dot system, and due to highly employed multilayer interconnection and shallow diffusion technique in process. ECL 100K features high integration and high speed owing to most advanced semiconductor manufacturing technique such as 3μm interconnection and oxidation film separation process, and, in addition features high reliability due to improvement of temperature compensation, voltage compensation and incorporation of know-how based on results and experiences from 10K. Fig. 5 shows cross-sectional structure of ECL 10K and ECL 100K.

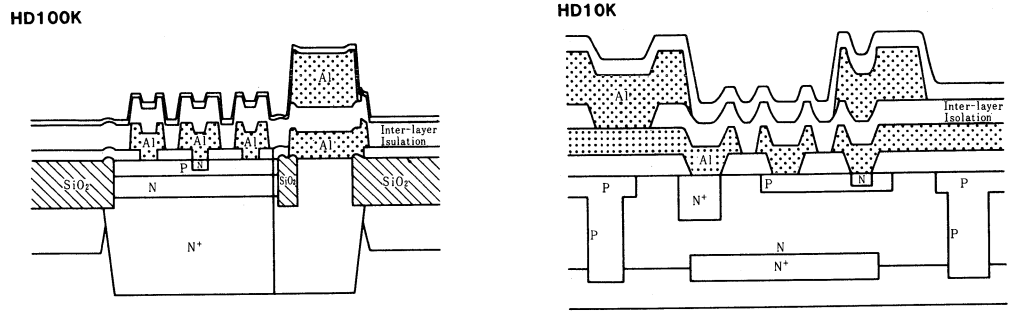


Fig.5 Cross-sectional Structure of ECL 10K and 100K

IC chips manufactured with most advanced technique are sealed into various types of packages. Major packages for ECL are Cerdip type, Flat packaged type and Ceramic type.

Recently, for high density assembly, LCC (leadless Chip Carrier) type is under development. These are all airtight seal type, and, because of their structure, these are suitable for high reliability equipments.

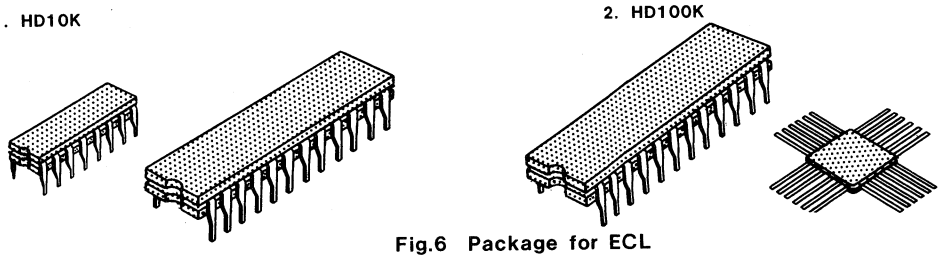


Fig.6 Package for ECL

5. RELIABILITY DATA

Examples of reliability test results at Hitachi are shown below.

5.1 Reliability data of ECL 100K

Reliability test data of HD100101, HD100130 and HD100160, as representative products of 100K, are shown in Table 2 and 3.

Table 2 Reliability Test Results of ECL100K (1)

Items	HD10010IF					
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*	
High Temperature Operation	$Ta=125°C$ $V_{EE}=-4.5V$	100pcs	3.7×10^5	0	2.5×10^{-6}	
	$Ta=150°C$ $V_{EE}=-4.5V$	100pcs	2.0×10^5	1 *1	1.0×10^{-5}	*1 Electrostatic destruction
High Temperature Storage	$Ta=150°C$	60pcs	1.2×10^4	0	7.7×10^{-6}	
	$Ta=200°C$	30pcs	6.0×10^4	0	1.5×10^{-5}	
Thermal Fatigue	$Ta=25°C$ $V_{EE}=-5.2V$ ON/OF= 10minutes/10minutes	40pcs	4×10^4 (cycles, pcs)	0	—	

* Reliability level 60%

Table 2 Reliability Test Results of ECL100K (2)

Items	HD100130F				
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-4.5V$	100pcs	1.0×10^5	0	9.2×10^{-6}
	$Ta=150°C$ $V_{EE}=-4.5V$	—	—	—	—
High Temperature Storage	$Ta=150°C$	—	—	—	—
	$Ta=200°C$	30pcs	3.0×10^4	0	3.1×10^{-5}
Thermal Fatigue	$Ta=25°C$ $V_{EE}=-5.2V$ ON/OF= 10minutes/10minutes	—	—	—	—

Table 2 Reliability Test Results of ECL100K (3)

Items	HD100160F				
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-4.5V$	—	—	—	—
	$Ta=150°C$ $V_{EE}=-4.5V$	100pcs	1.0×10^5	0	9.2×10^{-6}
High Temperature Storage	$Ta=150°C$	—	—	—	—
	$Ta=200°C$	30pcs	3.0×10^4	0	3.1×10^{-4}
Thermal Fatigue	$Ta=25°C$ $V_{EE}=-5.2V$ ON/OF= 10minutes/10minutes	50pcs	5×10^5 (cycles·pcs)	0	—

Table 2 Reliability Test Results of ECL100K (4)

Items	HD100101 (Cerdip)				
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-4.5V$	100pcs	2.0×10^5	0	4.6×10^{-6}
	$Ta=150°C$ $V_{EE}=-4.5V$	100pcs	2.0×10^5	0	4.6×10^{-6}
High Temperature Storage	$Ta=150°C$	50pcs	1.0×10^5	0	9.2×10^{-6}
	$Ta=200°C$	30pcs	6.0×10^4	0	1.5×10^{-5}
Thermal Fatigue	$Ta=25°C$ $V_{EE}=-5.2V$ ON/OF= 10minutes/10minutes	30pcs	3×10^4 (cycles·pcs)	0	—

* Reliability level 60%

Table 3 Reliability Test Results of ECL100K (1)

Items	Test Condition	HD100101/HD100130F		HD100101/HD100160 (Cerdip)	
		Number of Samples	Number of Failures	Number of Samples	Number of Failures
Temperature Cycle	−65°C ~ RT ~ +150°C 10cycles	100	0	100	0
Soldering Heat Resistivity	260°C, 10sec	50	0	50	0
Thermal Shock	0°C ~ 100°C 10cycles	50	0	50	0
Drop Shock	1,500G, 0.5ms 3times each on X, Y and Z	30	0	30	0
Variable Frequency Vibration	100~2,000Hz, 20G 3times each on X, Y and Z	30	0	30	0
Constant Acceleration	20,000G 1minute each on X, Y and Z	30	0	30	0

5.2 Reliability data of ECL 10K

Reliability test data of HD10101 and HD10136, as representative products of ECL 10K, are shown in Table 4 and 5.

Table 4 Reliability Test Results of ECL10K (1)

Items	HD10101				
	Test Condition	Number of Sambles	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-5.2V$	200pcs	4.5×10^5	0	2.3×10^{-6}
	$Ta=150°C$ $V_{EE}=-5.2V$	120pcs	2.4×10^5	0	3.8×10^{-6}
High Temperature Storage	$Ta=150°C$	38pcs	7.6×10^4	0	1.2×10^{-5}
	$Ta=200°C$	22pcs	4.4×10^4	0	2.1×10^{-5}

* Reliability level 60%

Reliability Test Results of ECL 10K (2)

Items	HD10136				
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-5.2V$	100pcs	2.0×10^5	0	4.6×10^{-6}
	$Ta=150°C$ $V_{EE}=-5.2V$	75pcs	1.5×10^5	0	6.1×10^{-6}
High Temperature Storage	$Ta=150°C$	38pcs	7.6×10^4	0	1.2×10^{-5}
	$Ta=200°C$	22pcs	4.4×10^4	0	2.1×10^{-4}

* Reliability level 60%

Table 5 Reliability Test Results of ECL 10K (1)

Items	Test Condition	HD10101		HD10136	
		Number of Samples	Number of Failures	Number of Samples	Number of Failures
Temperature Cycle	−65°C～RT～+150°C 10cycle	150	0	100	0
Soldering Heat Resistivity	260°C, 10sec.	22	0	22	0
Thermal Shock	0°C～100°C 10cycles	45	0	45	0
Drop Shock	1500G, 0.5ms 3 times each on X, Y and Z	38	0	38	0
Variable Frequency Vibration	100～2,000Hz, 20G 3 times each on X, Y and Z	38	0	38	0
Constant Acceleration	20,000G 1 minute each or X, Y and Z	38	0	38	0

5.3 Characteristics Change of ECL

Fundamental parameters of change in ECL are h_{FE} and I_{CBO} of transistors and parastic leak path. However, in device design, structures to suppress these degradations are employed and actual operating condition is chosen not to be affected by these degradations. Therefore, in the usual operating condition, characteristics degradation is hardly occured.

AC characteristics changes of HD100101 and HD10101 are shown in Fig. 7 and 8.

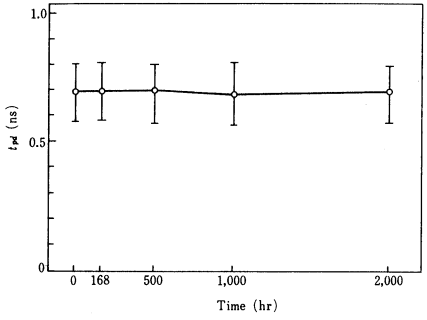


Fig.7 t_{pd} Change of HD100101

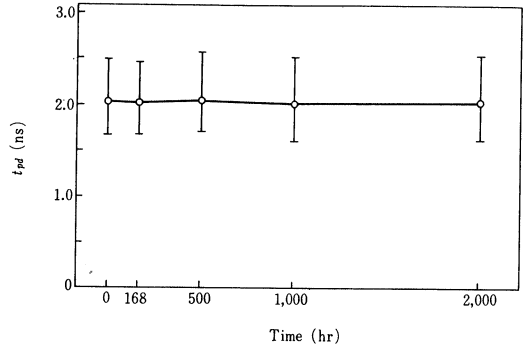


Fig.8 t_{pd} Change of HD10101

5.4 Field Failure Mode

Example of failures in fields are shown in Fig. 9 and 10.

Failure rate of ECL 10K is dereasing. However, because of using very fine lithographic technique, a percentage of failures caused by oxidation film pinhole, photoresist and foreign materials shows rather increase. In ECL 100K, by using high reliability process, the failures mentioned above are decreasing.

However, because finest lithographic technique in existing semiconductor manufacturing technique is used, ECL 100K is very sensitive to electrostatic charge. Therefore, treatments against electrostatic charge, same as MOS memories, are needed.

At Hitachi, in order to remove potential faults in manufacturing line, improvements of manufacturing process and 100% screening tests are carried out. In addition, analysis of failures occurred at customers' line and fields makes effective feedback to improvements of design and manufacturing.

Therefore, we appreciate very much for your cooperation in collecting data at customers' line and fields.

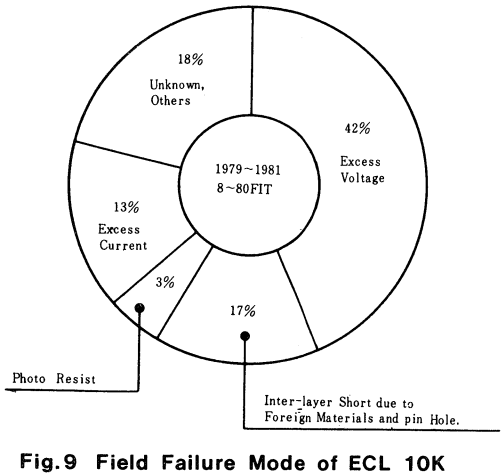


Fig.9 Field Failure Mode of ECL 10K

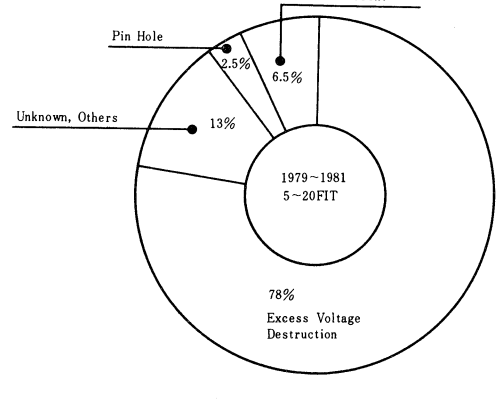


Fig.10 Field Failure Mode of ECL 100K

HANDLING PRECAUTIONS

High speed digital ICs feature high reliability owing to most advanced semiconductor manufacturing technique.
On the other hand, however, mishandling causes misoperation of the ICs or damage on them. Precautions in handling are described here hoping helpful to application design.

1. Precaution Against Electrostatic Charge

ECL 100K and 10K has less margin against electrostatic destruction due to double layer structure and shallow diffusion technique for high integration and high speed.
Therefore, more cautions than conventional products are needed for electrostatic charge. Followings are precautions in handling.

(1) At storage or transportation, in order for all IC pins to have same voltage level, please put ICs into conductive mat or pack in conductive magazine. An example of conductive mat in market is MOS PACK.
In the case that plastic magazine with conductive coating is used, effect against electrostatic charge decreases by using it many times. Therefore, aluminum magazine is recommended for using many times.

(2) Ground human body if ICs are touched with hand at board assembly or receiving inspection of ICs.

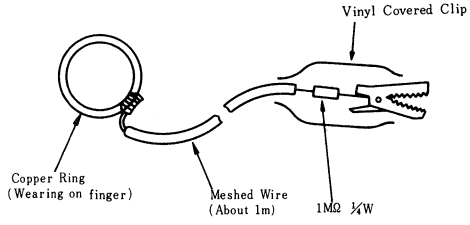


Fig.1 An Example of Grounding to Human Body

An example of grounding of human body is shown in Fig. 1. 1Mohms resistor is absolutely needed to avoid electrical shock.

(3) Keep relative humidity at 50% in the room. It prevents generation of electrostatic charge.

(4) Cloths are recommended to be like cotton which hardly generates electrostatic charge. Synthetic fiber cloths are not recommended.

(5) It is recommended to ground tip of solder iron. If possible, low voltage (12V or 24V) operation types are recommendable. Grounding of measurement equipments is absolutely necessary.

(6) At transportation of ICs in assembled board, it is recommended for packing material to be made of conductive sheets.

2. Prevention of Reverse Insertion of IC Pinouts

In the case of reverse insertion of IC pinouts to board, ICs which have symmetrical pinouts between V_{EE} and Ground causes high current flown. Interconnection on the chip is melted and device is destroyed. Precaution must be made even for the ICs which do not have symmetrical pinouts between V_{EE} and Ground, because excess current flows and sometimes device is destroyed.
On the device package, marking of No. 1 pin is stamped.
Please watch this marking and insert ICs properly.

3. Mounting and Removal of ICs during Voltage is Supplied

Usually, rather high current flows in regulator of ECL.
Therefore, if ICs are put in and pulled out to board during voltage is supplied, high voltage induced at current on/off destroys ICs. Mount and remove ICs after supply voltage is cut off.
Same precaution must be made in measurement with tester.

4. Prevention of Oscillation

ECL, especially 100K, has high cut-off frequency of transistor.
Therefore, sometimes, oscillation is caused in relation with external circuit, and misoperation of ICs is occured.
In such cases, about 0.1μF of capacitor, which has good high frequency characteristics, is recommended to put between ICs and voltage supply line.

5. Precaution on Simple "H" Level'

In some cases, it is seen that input of ICs is directly connected to ground to fix input as "H" level. However, it sometimes causes misoperation in conjunction with internal circuit composition.
"H" and "L" level of input are specified as $V_{IL(min)}$ and $V_{IH(max)}$ for ICs respectively. Please refer them and use ICs properly.

6. Cooling

Power dissipation of ECL is 90mW to 500mW in 10K, and 100mW to 700mW in 100K depending on products. In the case many ECLs are mounted on the board, natural convention is insufficient for cooling.

Therefore, please run forced air cooling with velocity higher than 2.5m/s. In addition, by cooling, improvement of reliability can be expected as shown in Fig. 2.

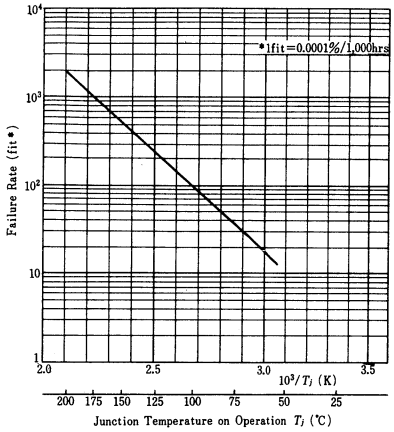


Fig. 2 Example of derating of ECL 10K

7. Other Precautions

(1) Deforming of magazine and carrier.

Since material of plastic magazine and carrier (for ECL 100K flat package) is usually thermal plasticity, they deforms at temperature higher than 40 to 50°C and may not perform sufficiently. If burn-in is carried out at users, please use aluminum magazine or other metal fixtures.

(2) Shock at transportation

Glass sealed type package is fragile. Usual handling and drop test (JIS C7021 A-8) on individual devices do not cause any problem.

However, it devices packed in magazine receive strong shock such as drop shock, devices hit neighbouring devices and packages may be damaged. Therefore, at transportation or loading on/off, be careful not to drop them. Even after devices are mounted on board, IC packages may be damaged if strength of board is not enough and board receives strong deforming stress. Please be careful on strength of board and handling. If any questions rose at using Hitachi products, please feel free to contact closest Hitachi representatives or offices.

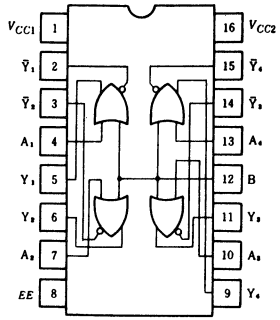
DATA SHEETS

HD10K Series

HD10101

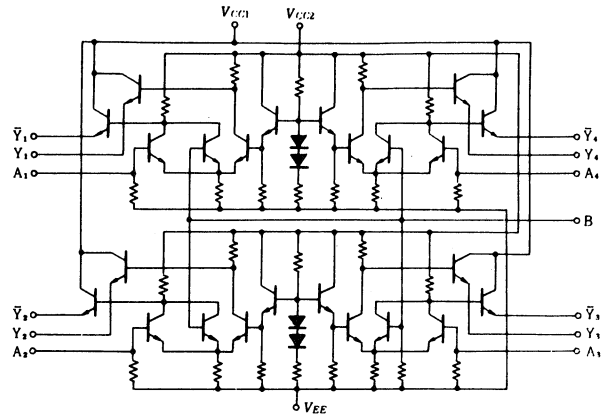
Quardruple OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	A input	25°C	—	—	265	μA
			B input		—	—	535	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

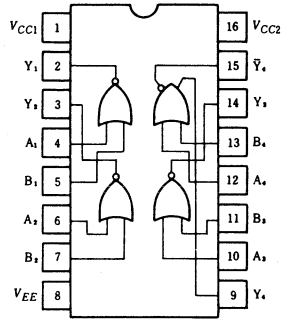
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

HD10102

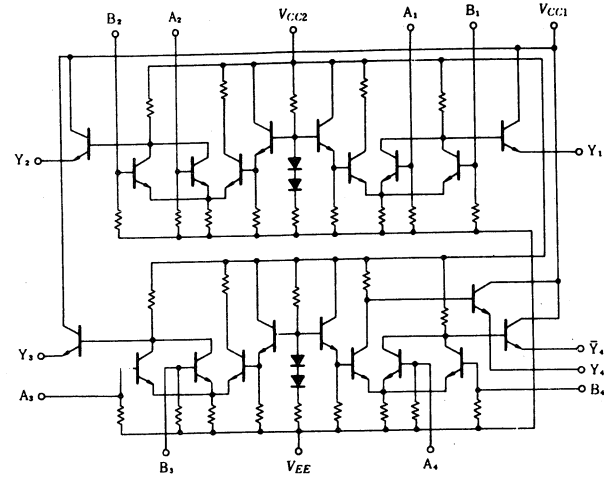
Quadruple 2-input NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

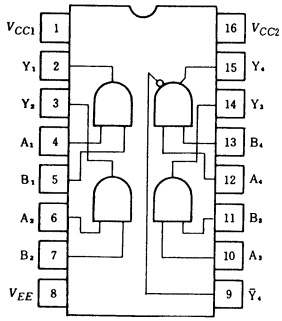
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

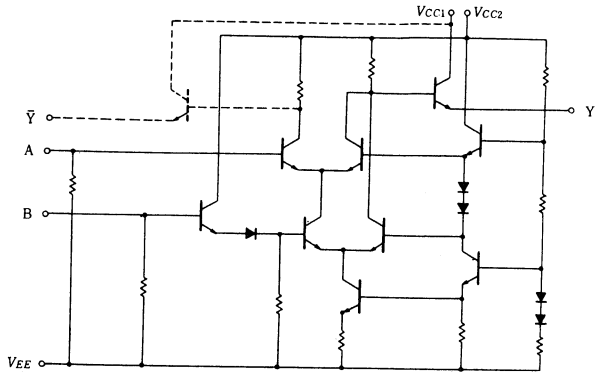
Quadruple 2-input AND Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC (1/4)



■DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	28	35	mA
Input Current	I_{IH}	V_{IH} = −0.810V, B input = −0.810V	A input	25°C	—	—	265	μA
		V_{IH} = −0.810V	B input		—	—	220	
	I_{IL}	V_{IL} = −1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V		25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V		−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V		25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IH} = −0.890V, V_{IHA} = −1.205V or V_{ILA} = −1.500V		−30°C	−1.080	—	—	V
		V_{IH} = −0.810V, V_{IHA} = −1.105V or V_{ILA} = −1.475V		25°C	−0.980	—	—	
		V_{IH} = −0.700V, V_{IHA} = −1.035V or V_{ILA} = −1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IH} = −0.890V, V_{IHA} = −1.205V		−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IH} = −0.810V, V_{IHA} = −1.105V		25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IH} = −0.700V, V_{IHA} = −1.105V		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

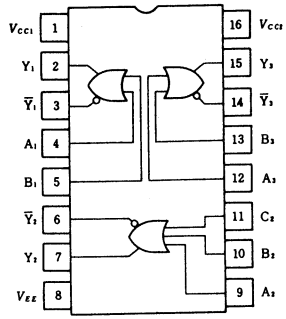
Item	Symbol	Test Condition			min	typ	max	Unit
Propagation Delay Time	t_{PLH}	A input	R_L = 50Ω	−30°C	1.0	—	4.3	ns
				25°C	1.0	2.2	4.0	
				85°C	1.0	—	4.2	
		B input		−30°C	1.0	—	4.3	
				25°C	1.0	2.7	4.0	
				85°C	1.0	—	4.2	
	t_{PHL}	A input		−30°C	1.0	—	4.3	ns
				25°C	1.0	2.2	4.0	
				85°C	1.0	—	4.2	
		B input		−30°C	1.0	—	4.3	
				25°C	1.0	2.7	4.0	
				85°C	1.0	—	4.2	
Rise/Fall Time	t_{TLH}	A, B input		−30°C	1.5	—	3.7	ns
				25°C	1.5	2.0	3.5	
				85°C	1.5	—	3.6	
	t_{THL}			−30°C	1.5	—	3.7	ns
				25°C	1.5	2.0	3.5	
				85°C	1.5	—	3.6	

Note) Please refer to test circuit and waveform of common item.

HD10105

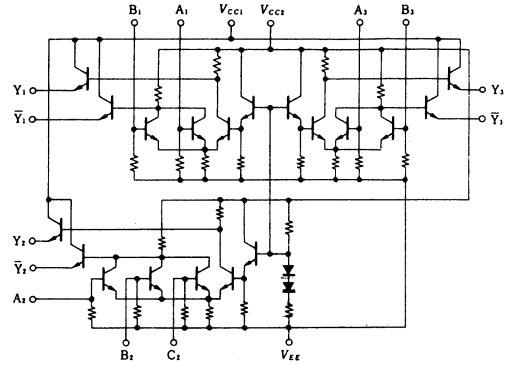
Triple 2-3-2-input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	17	21	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

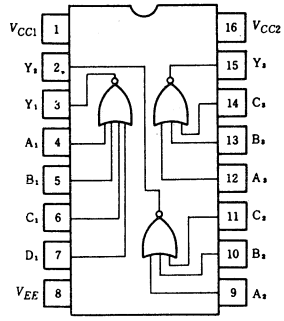
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

HD10106

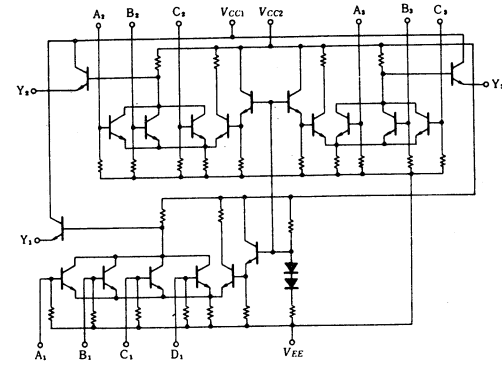
Triple 4-3-3-input NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	17	21	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{IHA}=-1.035V$	85°C	—	—	−1.595	

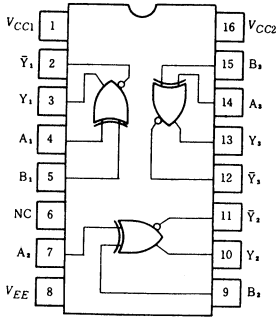
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=-2.0V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

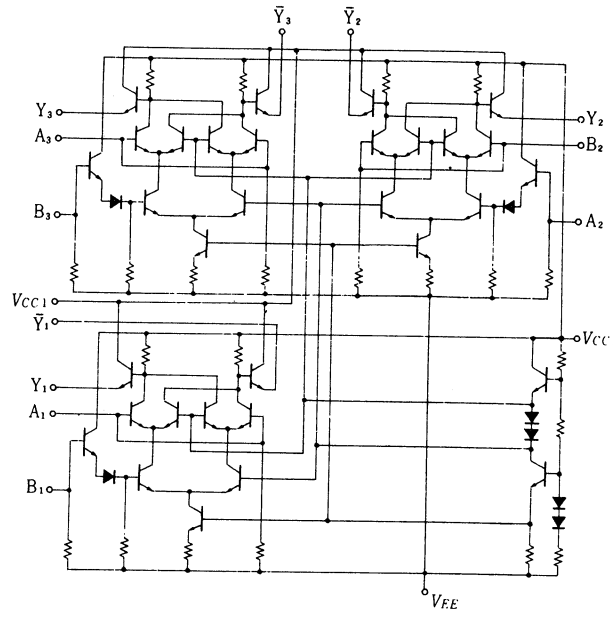
Triple 2-input Exclusive-OR/Exclusive-NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All inputs = −0.810V		25°C	—	—	28	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	A input	25°C	—	—	265	μA
			B input		—	—	220	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

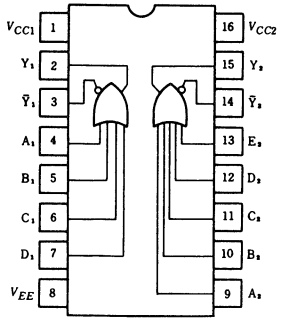
■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Propagation Delay Time	t_{PLH}	A input	R_L=50Ω	−30°C	1.1	—	3.8	ns
				25°C	1.1	2.0	3.7	
				85°C	1.1	—	4.0	
		B input		−30°C	1.1	—	3.8	
				25°C	1.1	2.8	3.7	
				85°C	1.1	—	4.0	
	t_{PHL}	A input		−30°C	1.1	—	3.8	ns
				25°C	1.1	2.0	3.7	
				85°C	1.1	—	4.0	
		B input		−30°C	1.1	—	3.8	
				25°C	1.1	2.8	3.7	
				85°C	1.1	—	4.0	
Rise/Fall Time	t_{TLH}	A, B input		−30°C	1.1	—	3.5	ns
				25°C	1.1	2.5	3.5	
				85°C	1.1	—	3.8	
	t_{THL}			−30°C	1.1	—	3.5	ns
				25°C	1.1	2.5	3.5	
				85°C	1.1	—	3.8	

Note) Please refer to test circuit and waveform of common item.

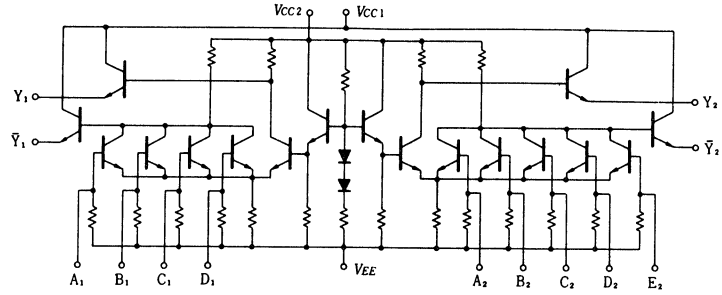
Dual 4-5-input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	11	14	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

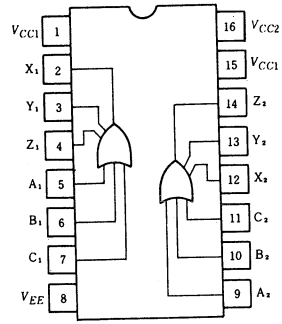
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

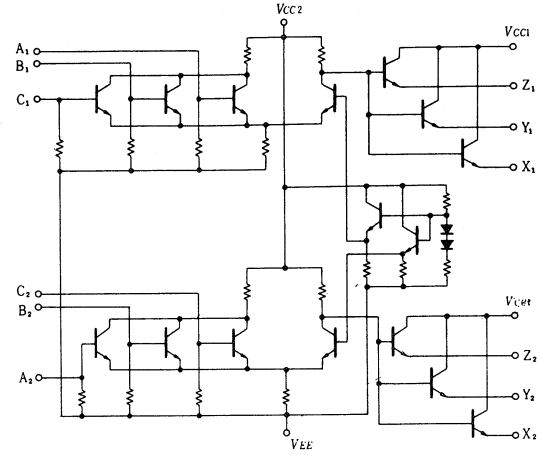
Dual 3-input 3-output OR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	30	38	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	425	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

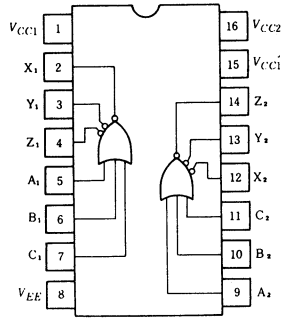
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.5	ns
			25°C	1.4	2.4	3.5	
			85°C	1.5	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.5	ns
			25°C	1.4	2.4	3.5	
			85°C	1.5	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	1.0	—	3.5	ns
			25°C	1.1	2.2	3.5	
			85°C	1.2	—	3.8	
	t_{THL}		−30°C	1.0	—	3.5	ns
			25°C	1.1	2.2	3.5	
			85°C	1.2	—	3.8	

Note) Please refer to test circuit and waveform of common item.

HD10111

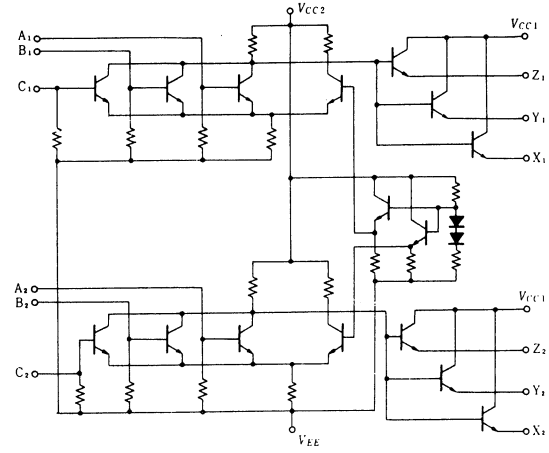
Dual 3-input 3-output NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	—	38	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	425	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{IHA}=-1.035V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

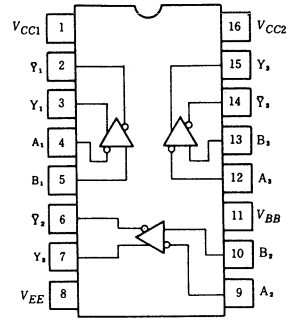
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.5	ns
			25°C	1.4	2.4	3.5	
			85°C	1.5	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.5	ns
			25°C	1.4	2.4	3.5	
			85°C	1.5	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	1.0	—	3.5	ns
			25°C	1.1	2.2	3.5	
			85°C	1.2	—	3.8	
	t_{THL}		−30°C	1.0	—	3.5	ns
			25°C	1.1	2.2	3.5	
			85°C	1.2	—	3.8	

Note) Please refer to test circuit and waveform of common item.

Triple Line Receivers

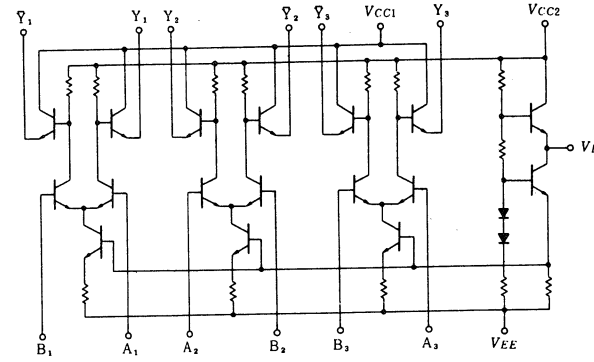
The HD10116 is designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current source provides these receivers with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent upsetting the current source bias network.

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}*		25°C	—	17	21	mA
Input Current	I_{IH}**	$V_{IH}=-0.810V$	25°C	—	—	95	μA
	I_{CBO}**	$V_{IN}=-5.2V$	25°C	—	—	1.0	μA
Output Voltage	V_{OH}***	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}***	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}***	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}***	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	
Reference Voltage	V_{BB}		−30°C	−1.420	—	−1.280	V
			25°C	−1.350	—	−1.230	
			85°C	−1.295	—	−1.150	

* Bn input is connected to V_{BB} and V_{IL} min is supplied to An input.
** Bn input is connected to V_{BB} and V_{IL} min is supplied to A input.
*** Other inputs are connected to V_{BB} and each one input of other receiver is connected to V_{BB}.

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L=50Ω, Other inputs = V_{BB}	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.1	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.1	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

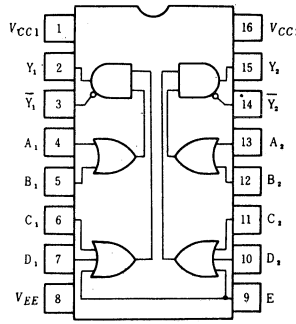
HD10117

Dual 2-wide 2-3-input OR-AND/OR-AND-INVERT Gates

The HD10117 is designed for use as a data control of digital Multiplexer, data distribution and etc..

The E input (pin 9) is common input of dual gates.

■PIN ARRANGEMENT



(Top View)

■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	E input	25°C	—	—	350	μA
			Other inputs		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

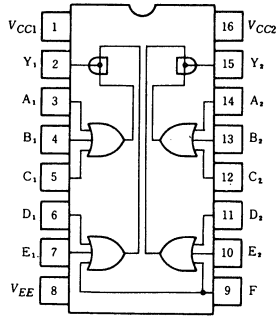
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	0.9	—	4.1	ns
			25°C	1.1	2.2	4.0	
			85°C	1.1	—	4.6	
	t_{THL}		−30°C	0.9	—	4.1	ns
			25°C	1.1	2.2	4.0	
			85°C	1.1	—	4.6	

Note) Please refer to test circuit and waveform of common item.

HD10118

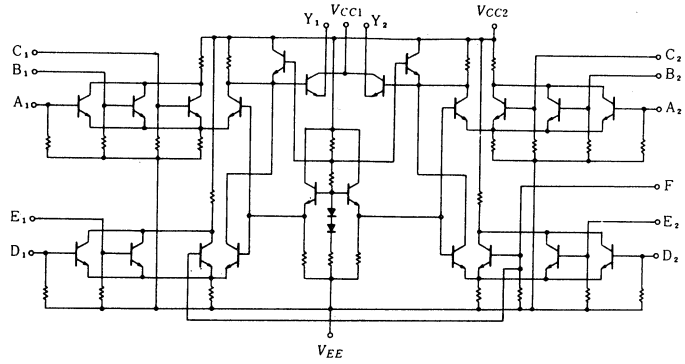
Dual 2-wide 3-input OR-AND Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	F input	25°C	—	—	370	μA
			Other inputs		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$		−30°C	−2.000	—	−1.675	V
		$V_{IL}=-1.850V$		25°C	−1.990	—	−1.650	
		$V_{IL}=-1.825V$		85°C	−1.920	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

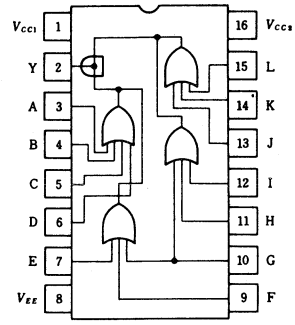
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	0.8	—	4.1	ns
			25°C	1.5	2.5	4.0	
			85°C	1.5	—	4.6	
	t_{THL}		−30°C	0.8	—	4.1	ns
			25°C	1.5	2.5	4.0	
			85°C	1.5	—	4.6	

Note) Please refer to test circuit and waveform of common item.

HD10119

4-wide 4-3-3-3-input OR-AND Gate

■PIN ARRANGEMENT



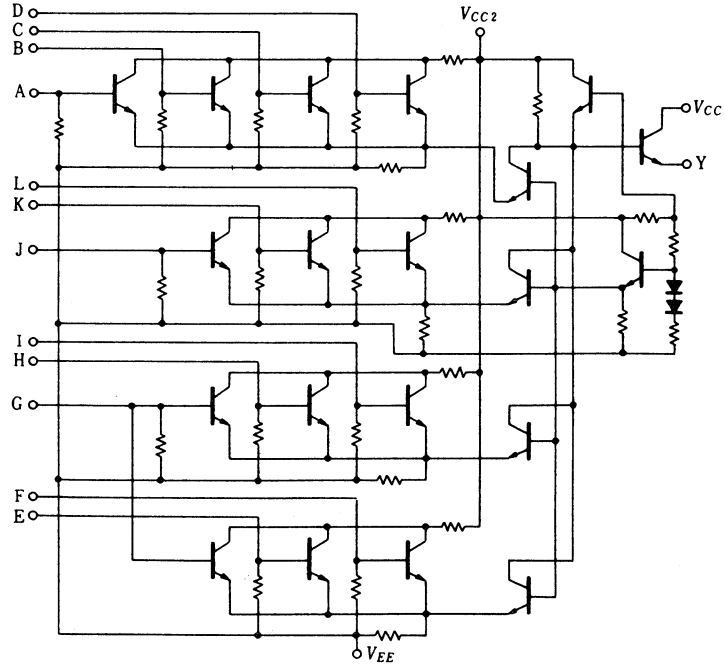
(Top View)

■FUNCTION TABLE

Inputs												Outputs
A	B	C	D	E	F	G	H	I	J	K	L	Y
L	L	L	L	×	×	×	×	×	×	×	×	L
×	×	×	×	L	L	L	×	×	×	×	×	L
×	×	×	×	×	×	L	L	L	×	×	×	L
×	×	×	×	×	×	×	×	×	L	L	L	L
Notes 1												H

Notes) 1. Each input of OR gates are combined to high.
2. X: Don't Care

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	G input	25°C	—	—	370	μA
			Other inputs		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

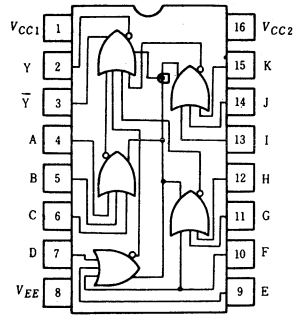
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	0.8	—	4.1	ns
			25°C	1.5	2.5	4.0	
			85°C	1.5	—	4.6	
	t_{THL}		−30°C	0.8	—	4.1	ns
			25°C	1.5	2.5	4.0	
			85°C	1.5	—	4.6	

Note) Please refer to test circuit and waveform of common item.

HD10121

4-wide OR-AND/OR-AND-INVERT Gate

■PIN ARRANGEMENT



(Top View)

■DC CHARACTERISTICS (V_{EE}=−5.2V, Ta=−30~+85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	V_{IH}=−0.810V	F input	25°C	—	—	370	μA
			Other inputs		—	—	265	
	I_{IL}	V_{IL}=−1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH}=−0.890V or V_{IL}=−1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH}=−0.810V or V_{IL}=−1.850V		25°C	−0.960	—	−0.810	
		V_{IH}=−0.700V or V_{IL}=−1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL}=−1.890V or V_{IH}=−0.890V		−30°C	−1.890	—	−1.675	V
		V_{IL}=−1.850V or V_{IH}=−0.810V		25°C	−1.850	—	−1.650	
		V_{IL}=−1.825V or V_{IH}=−0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA}=−1.205V or V_{ILA}=−1.500V		−30°C	−1.080	—	—	V
		V_{IHA}=−1.105V or V_{ILA}=−1.475V		25°C	−0.980	—	—	
		V_{IHA}=−1.035V or V_{ILA}=−1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{ILA}=−1.500V or V_{IHA}=−1.205V		−30°C	—	—	−1.655	V
		V_{ILA}=−1.475V or V_{IHA}=−1.105V		25°C	—	—	−1.630	
		V_{ILA}=−1.440V or V_{IHA}=−1.035V		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE}=−3.2V, V_{CC}=+2.0V, Ta=−30~+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L=50Ω	−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	0.9	—	4.1	ns
			25°C	1.1	2.5	4.0	
			85°C	1.1	—	4.6	
	t_{THL}		−30°C	0.9	—	4.1	ns
			25°C	1.1	2.5	4.0	
			85°C	1.1	—	4.6	

Note) Please refer to test circuit and waveform of common item.

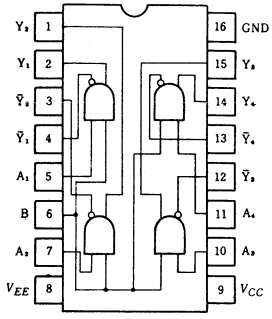
Quadruple TTL to ECL Translators

The HD10124 is a quad translator for interfacing data and control signals between a saturated logic section and the ECL section of digital systems. The device has TTL compatible inputs, and ECL complementary open-emitter outputs that allow use as an inverting/noninverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a ECL high logic state.

Power supply requirements are ground, +5.0V, and −5.2V. The DC levels are standard or Schottky TTL in, ECL 10K out.

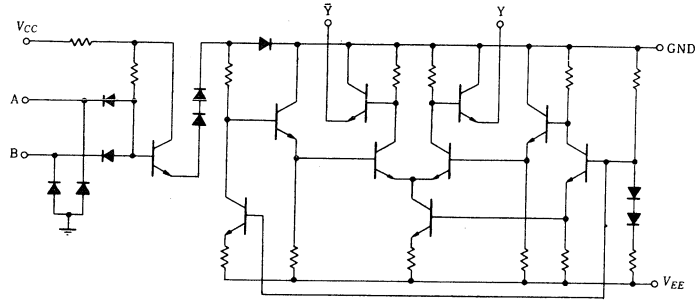
An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the ECL equipment, where the signal can be received by any of the ECL receivers or the HD10125 ECL to TTL translator.

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



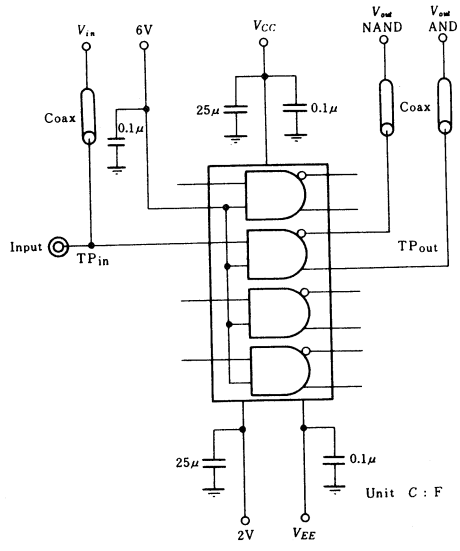
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $V_{CC}=+5.0V$, $Ta=-30\sim+85°C$)

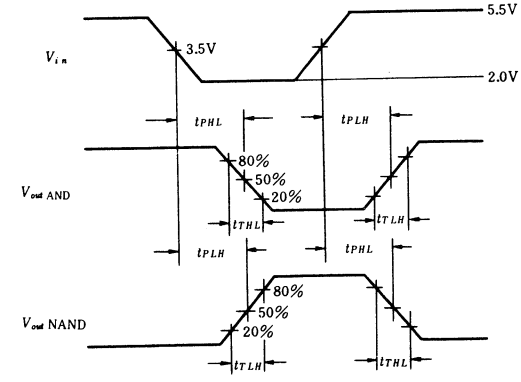
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	—	66	mA
	I_{CCH}	All inputs=4V		25°C	—	—	16	mA
	I_{CCL}	All inputs=0V		25°C	—	—	25	mA
Input Current	I_{IH}	$V_{IN}=2.4V$, Other inputs=0.4V	A input	25°C	—	—	50	μA
			B input		—	—	200	
	I_{IL}	$V_{IN}=0.4V$, Other inputs=4V	A input	25°C	−3.2	—	—	mA
			B input		−12.8	—	—	
	I_I	$V_{IN}=5.5V$, Other inputs=0V		25°C	—	—	1	mA
Input Clamp Voltage	V_{IK}	$I_{IN}=-10mA$, Other inputs open		25°C	−1.5	—	—	V
Output Voltage	V_{OH}	$V_{IH}=4V$ or $V_{IL}=0.4V$		−30°C	−1.060	—	−0.890	V
				25°C	−0.960	—	−0.810	
				85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=4V$ or $V_{IL}=0.4V$		−30°C	−1.890	—	−1.675	V
				25°C	−1.850	—	−1.650	
				85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=2.0V$ or $V_{ILA}=1.10V$		−30°C	−1.080	—	—	V
		$V_{IHA}=1.80V$ or $V_{ILA}=1.10V$		25°C	−0.980	—	—	
		$V_{IHA}=1.80V$ or $V_{ILA}=0.90V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=1.10V$ or $V_{IHA}=2.0V$		−30°C	—	—	−1.655	V
		$V_{ILA}=1.10V$ or $V_{IHA}=1.80V$		25°C	—	—	−1.630	
		$V_{ILA}=0.90V$ or $V_{IHA}=1.80V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE}=−3.2V, V_{CC}=+7.0V, GND=+2.0V, Ta=−30~+85°C)

Item		Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	In-phase	t_{PLH}	R_L=50Ω	−30°C	1.0	—	6.8	ns
				25°C	1.5	3.5	6.0	
				85°C	1.0	—	6.8	
		t_{PHL}		−30°C	1.0	—	6.8	ns
				25°C	1.5	3.5	6.0	
				85°C	1.0	—	6.8	
	Out-of-phase	t_{PLH}		−30°C	1.0	—	6.0	ns
				25°C	1.5	3.5	6.0	
				85°C	1.5	—	6.8	
		t_{PHL}		−30°C	1.5	—	6.8	ns
				25°C	1.5	3.5	6.0	
				85°C	1.0	—	6.0	
Rise/Fall Time		t_{TLH}		−30°C	1.0	—	4.2	ns
				25°C	1.1	2.5	3.9	
				85°C	1.1	—	4.3	
		t_{THL}		−30°C	1.0	—	4.2	ns
				25°C	1.1	2.5	3.9	
				85°C	1.1	—	4.3	

■TEST CIRCUIT





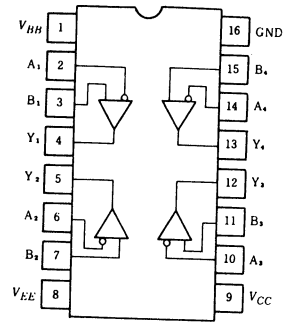
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Input Pulse; t_{TLH}=t_{THL}=5.5±0.5ns (10 to 90%)
4. Unused outputs connected to a 50Ω resistor to ground.

HD10125

Quadruple ECL to TTL Translators

The HD10125 is a quad translator for interfacing data and control signals between the ECL section and saturated logic sections of digital systems. The HD10125 incorpolates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/ noninverting translator or as a differential line receiver.
The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs go to a low logic level whenever the inputs are left floating. Power supply requirements are ground, +5V and −5.2V. The HD10125 has a fanout of 10 TTL loads. The DC levels are ECL 10K in and Schottky TTL or standard TTL out. The device has an input common mode noise rejection of ±1.0V.

■PIN ARRANGEMENT



(Top View)

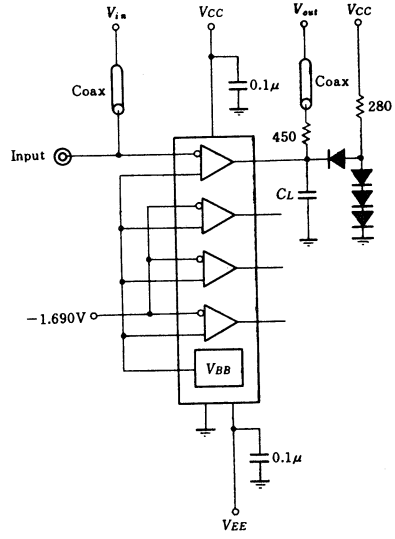
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $V_{CC}=+5.0V$, $Ta=-30\sim+85°C$)

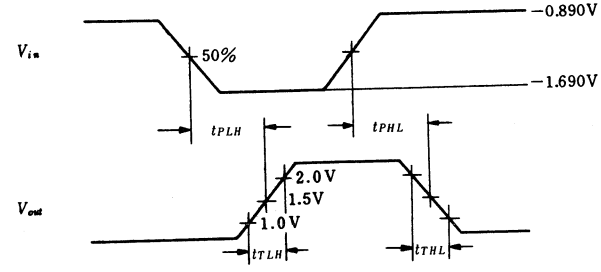
Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	—	40	mA
	I_{CCH}	$V_{IH}=-0.810V$	25°C	—	—	52	mA
	I_{CCL}	$V_{IL}=-1.850V$	25°C	—	—	39	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	115	μA
	I_{CBO}	$V_{IN}=-5.2V$	25°C	—	—	1.0	μA
Output Voltage	V_{OH}	$V_{IL}=-1.890V$, $I_{OH}=-2mA$	−30°C	2.5	—	—	V
		$V_{IL}=-1.850V$, $I_{OH}=-2mA$	25°C	2.5	—	—	
		$V_{IL}=-1.825V$, $I_{OH}=-2mA$	85°C	2.5	—	—	
	V_{OL}	$V_{IH}=-0.890V$, $I_{OL}=$ mA	−30°C	—	—	0.5	V
		$V_{IH}=-0.810V$, $I_{OL}=20mA$	25°C	—	—	0.5	
		$V_{IH}=-0.700V$, $I_{OL}=20mA$	85°C	—	—	0.5	
Output Threshold Voltage	V_{OHA}	$V_{ILA}=-1.500V$, $I_{OH}=-2mA$	−30°C	2.5	—	—	V
		$V_{ILA}=-1.475V$, $I_{OH}=-2mA$	25°C	2.5	—	—	
		$V_{ILA}=-1.440V$, $I_{OH}=-2mA$	85°C	2.5	—	—	
	V_{OLA}	$V_{IHA}=-1.205V$, $I_{OL}=20mA$	−30°C	—	—	0.5	V
		$V_{IHA}=-1.105V$, $I_{OL}=20mA$	25°C	—	—	0.5	
		$V_{IHA}=-1.035V$, $I_{OL}=20mA$	85°C	—	—	0.5	
Indeterminate Input Protection Test	V_{OLS1}	$V_{IN}=V_{EE}$, $I_{OL}=20mA$	−30°C	—	—	0.5	V
			25°C	—	—	0.5	
			85°C	—	—	0.5	
	V_{OLS2}	$I_{OL}=20mA$	−30°C	—	—	0.5	V
			25°C	—	—	0.5	
			85°C	—	—	0.5	
Output Short-circuit Current	I_{OS}	A input=−1.850V, B input=V_{BB}	25°C	40	—	100	mA
Reference Voltage	V_{BB}	A input=−1.890V, B input=V_{BB}	−30°C	−1.420	—	−1.280	V
		A input=−1.850V, B input=V_{BB}	25°C	−1.350	—	−1.230	
		A input=−1.825V, B input=V_{BB}	85°C	−1.295	—	−1.150	
Common Mode Rejection Test	V_{OH}	A input=−0.890V or −2.890V, B input=+0.110V or −1.890V, $I_{OH}=-2mA$	−30°C	2.5	—	—	V
		A input=−0.850V or −2.850V, B input=+0.190V or −1.810V, $I_{OH}=-2mA$	25°C	2.5	—	—	
		A input=−0.825V or −2.825V, B input=+0.300V or −1.700V, $I_{OH}=-2mA$	85°C	2.5	—	—	
	V_{OL}	A input=+0.110V or −1.890V, B input=−0.890V or −2.890V, $I_{OL}=20mA$	−30°C	—	—	0.5	V
		A input=+0.190V or −1.810V, B input=−0.850V or −2.850V, $I_{OL}=20mA$	25°C	—	—	0.5	
		A input=+0.300V or −1.700V, B input=−0.825V or −2.825V, $I_{OL}=20mA$	85°C	—	—	0.5	

■AC CHARACTERISTICS (V_{EE}=−5.2V, V_{CC}=+5.0V, Ta=−30~+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L=280Ω, C_L=25pF	−30°C	1.0	—	6.0	ns
			25°C	1.0	4.5	6.0	
			85°C	1.0	—	6.0	
	t_{PHL}		−30°C	1.0	—	6.0	ns
			25°C	1.0	4.5	6.0	
			85°C	1.0	—	6.0	
Rise/Fall Time	t_{TLH}		−30°C	—	—	3.3	ns
			25°C	—	—	3.3	
			85°C	—	—	3.3	
	t_{THL}		−30°C	—	—	3.3	ns
			25°C	—	—	3.3	
			85°C	—	—	3.3	

■TEST CIRCUIT



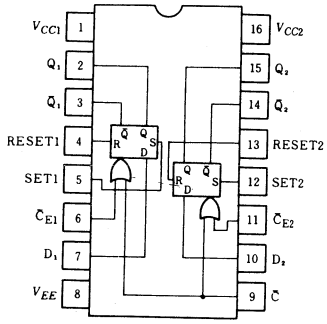


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be 6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. C_L=25pF, including test fixture.
4. For single-ended input testing, one input from each gate must be tied to V_{BB} (pin 1).

Dual D-type Latches

The HD10130 is a clocked dual D-type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode the enable inputs perform the function of controlling the common clock($\overline{C}$). Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state a change in the information present at the data inputs will not affect the output information. The set and reset inputs for not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

■PIN ARRANGEMENT



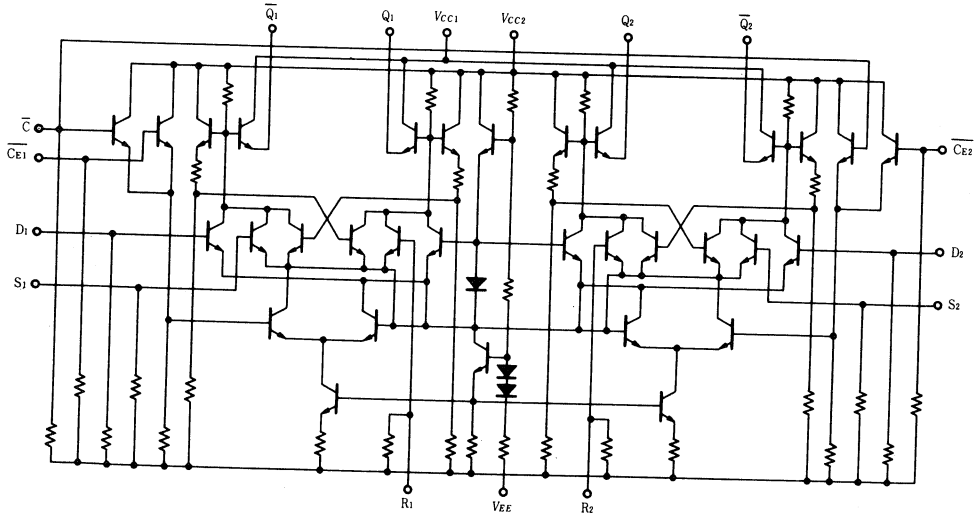
(Top View)

■FUNCTION TABLE

D	$\overline{C}$	$\overline{C}_E$	Q_{n+1}
L	L	L	L
H	L	L	H
×	L	H	Q_n
×	H	L	Q_n
×	H	H	Q_n

× : Don't care.

■CIRCUIT SCHEMATIC



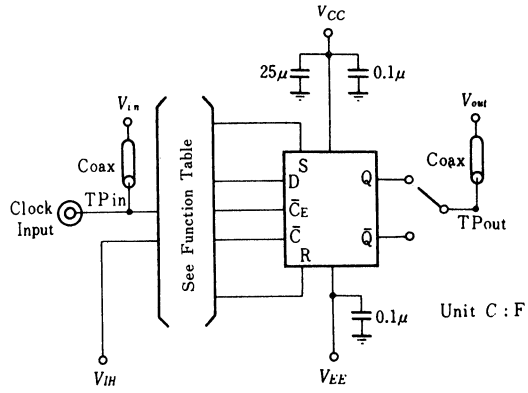
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85℃$)

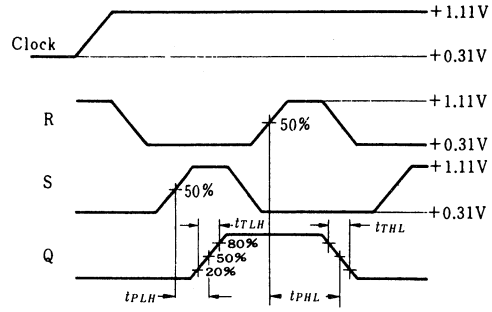
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	30	35	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	$\overline{C_E}$	25℃	—	—	220	μA
			$\overline{C}$		—	—	265	
			R, S, $\overline{C}$		—	—	285	
		$V_{IH}=-0.810V$, $\overline{C}=-1.850V$	D, S		—	—	285	
	I_{IL}	$V_{IL}=-1.850V$		25℃	—	—	0.5	μA
Output Voltage	V_{OH}	S=−0.890V		−30℃	−1.060	—	−0.890	V
		S=−0.810V		25℃	−0.960	—	−0.810	
		S=−0.700V		85℃	−0.890	—	−0.700	
	V_{OL}	R=−0.890V		−30℃	−1.890	—	−1.675	V
		R=−0.810V		25℃	−1.850	—	−1.650	
		R=−0.700V		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$\overline{C}=-1.890V$, D=−1.205V		−30℃	−1.080	—	—	V
		$\overline{C}=-1.850V$, D=−1.105V		25℃	−0.980	—	—	
		$\overline{C}=-1.825V$, D=−1.035V		85℃	−0.910	—	—	
	V_{OLA}	$\overline{C}=-1.890V$		−30℃	—	—	−1.655	V
		$\overline{C}=-1.850V$		25℃	—	—	−1.630	
		$\overline{C}=-1.825V$		85℃	—	—	−1.595	

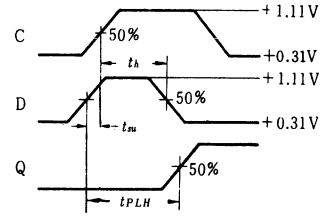
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85℃$)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	D	Q, $\overline{Q}$	$R_L=50Ω$	−30℃	1.0	—	3.6	ns
					25℃	1.0	2.5	3.5	
					85℃	1.0	—	3.8	
	t_{PHL}				−30℃	1.0	—	3.6	ns
					25℃	1.0	2.5	3.5	
					85℃	1.0	—	3.8	
	t_{PLH}	S, R	Q, $\overline{Q}$		−30℃	1.0	—	3.6	ns
					25℃	1.0	2.7	3.5	
					85℃	1.1	—	3.9	
	t_{PHL}				−30℃	1.0	—	3.6	ns
					25℃	1.0	2.7	3.5	
					85℃	1.1	—	3.9	
	t_{PLH}	$\overline{C_E}$	Q, $\overline{Q}$		−30℃	1.0	—	4.3	ns
					25℃	1.0	—	4.0	
					85℃	1.0	—	4.1	
	t_{PHL}				−30℃	1.0	—	4.3	ns
					25℃	1.0	—	4.0	
					85℃	1.0	—	4.1	
Rise/Fall Time	t_{TLH}	D	Q, $\overline{Q}$		−30℃	1.0	—	3.6	ns
					25℃	1.1	2.7	3.5	
					85℃	1.1	—	3.8	
	t_{THL}				−30℃	1.0	—	3.6	ns
					25℃	1.1	2.7	3.5	
					85℃	1.1	—	3.8	
Setup Time	t_{su}	$\overline{C_E}$, D	Q, $\overline{Q}$		25℃	—	—	2.5	ns
Hold Time	t_h				25℃	—	—	1.5	ns

TEST CIRCUIT







Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

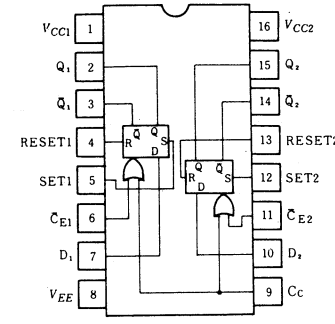
HD10131

Dual D-type Master-Slave Flip Flops

The HD10131 is a dual master-slave type D flip-flop. Asynchronous Set(S) and Reset(R) override Clock(C_C) and Clock Enable($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data(D) input will not affect the output information at any other time due to master-slave construction.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

●R-S

R	S	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	Q_n	$\overline{Q}_n$
L	H	H	L
H	L	L	H
H	H	×	×

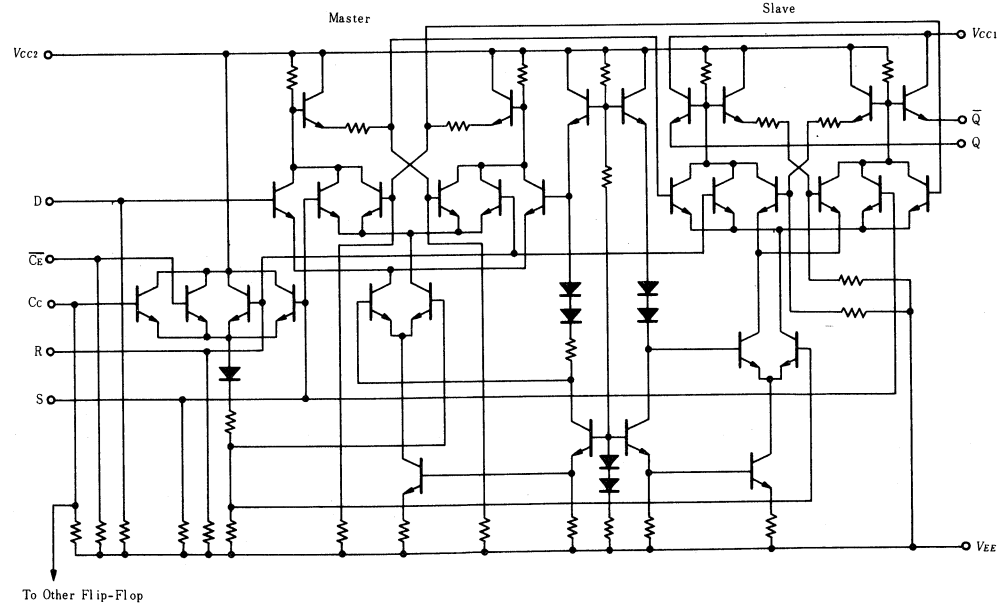
× : Not Defined.

●Clock

C	D	Q_{n+1}
L	×	Q_n
↑	L	L
↑	H	H

Notes) 1. Don't Care
2. $C=\overline{CE}+C_C$
3. A ↑ is a clock transition from a low to a high state.

■CIRCUIT SCHEMATIC



DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

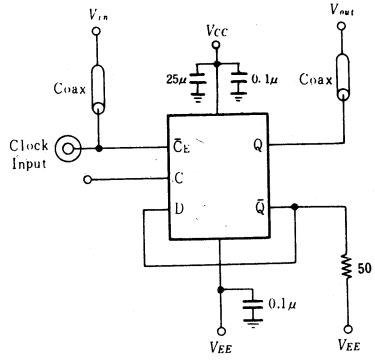
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	45	56	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	R, S	25°C	—	—	330	μA
			$\overline{C_E}$		—	—	220	
			D		—	—	245	
			C_C		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

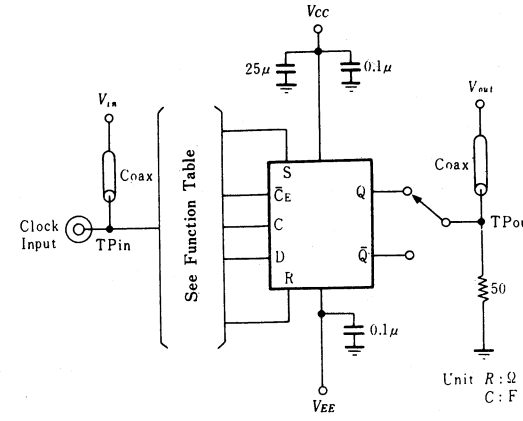
Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	C_C, $\overline{C_E}$	Q, $\overline{Q}$	$R_L=50\Omega$	−30°C	1.4	—	4.6	ns
					25°C	1.5	3.0	4.5	
					85°C	1.5	—	5.0	
	t_{PHL}				−30°C	1.4	—	4.6	ns
					25°C	1.5	3.0	4.5	
					85°C	1.5	—	5.0	
	t_{PLH}	R, S	Q, $\overline{Q}$		−30°C	1.1	—	4.4	ns
					25°C	1.2	2.8	4.3	
					85°C	1.2	—	4.8	
	t_{PHL}				−30°C	1.1	—	4.4	ns
					25°C	1.2	2.8	4.3	
					85°C	1.2	—	4.8	
Rise/Fall Time	t_{TLH}	C_C, $\overline{C_E}$	Q, $\overline{Q}$		−30°C	1.0	—	4.6	ns
					25°C	1.1	2.5	4.5	
					85°C	1.1	—	4.9	
	t_{THL}				−30°C	1.0	—	4.6	ns
					25°C	1.1	2.5	4.5	
					85°C	1.1	—	4.9	
Setup Time	t_{su}	$\overline{C_E}$, D	Q, $\overline{Q}$		25°C	—	—	2.5	ns
Hold Time	t_h				25°C	—	—	1.5	ns
Max. Toggle Frequency	f_{Tog}	$\overline{C_E}$	Q, $\overline{Q}$		−30°C	125	—	—	MHz
					25°C	125	160	—	
					85°C	125	—	—	

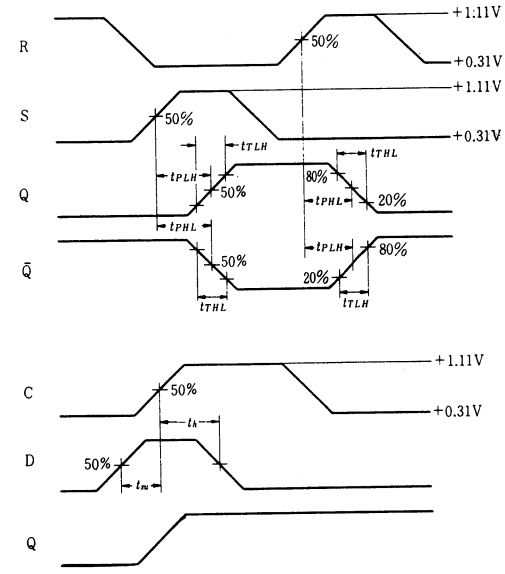
■AC CHARACTERISTIC TEST CIRCUITS

1. Toggle Frequency



2. Switching Time





Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition unchanged at the data.

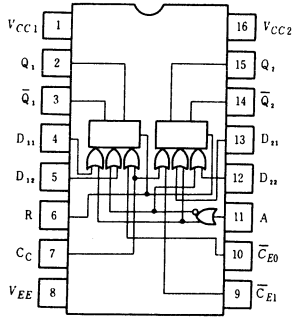
Dual Multiplexers (with Latch and common Reset)

The HD10132 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to used to clock the latch, the clock enable($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock(C_C). The data select(A) input determines which data input is enabled. A high(H) level enables data inputs D12 and D22 and a low(L) level enables data inputs D11 and D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state a change in the information present at the data inputs will not affect the output information.

The reset input is enabled when the clock is in the high state and disabled when the clock is in the high state, and disabled when the clock is low.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

R	D	C_C	$\overline{C_E}$	Q_{n+1}
×	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
×	H	L	L	H
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	×	×	H	L

Notes) 1. Don't care.
2. $Dn=(\overline{A}\cdot Dn_1)+(A\cdot Dn_2)$

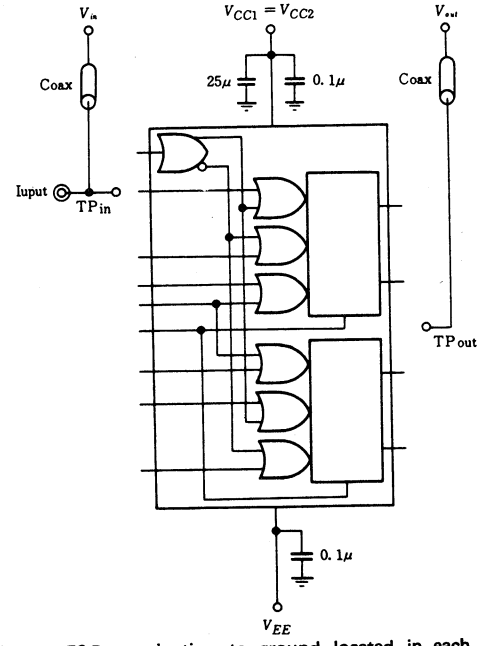
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

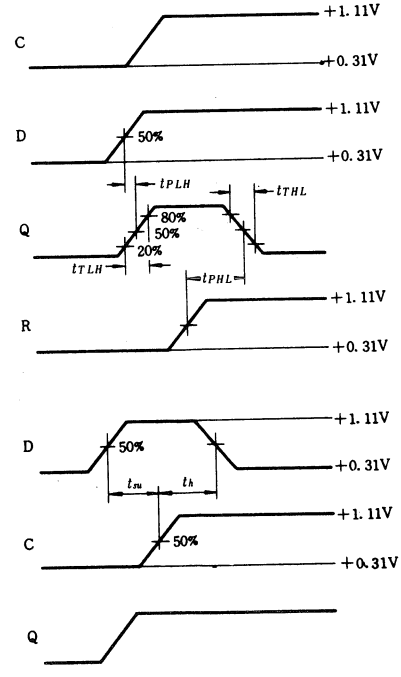
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	44	55	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	D, C_C	25°C	—	—	290	μA
			R		—	—	390	
			$\overline{C_E}$, A		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	D	Q, $\overline{Q}$	R_L=50Ω	1.0	—	3.3	ns
	t_{PHL}				1.0	—	3.3	ns
	t_{PLH}	R	Q, $\overline{Q}$		1.0	—	3.8	ns
	t_{PHL}				1.0	—	3.8	ns
	t_{PLH}	Cc	Q, $\overline{Q}$		1.0	—	5.7	ns
	t_{PHL}				1.0	—	5.7	ns
	t_{PLH}	A	Q, $\overline{Q}$		1.0	—	4.6	ns
	t_{PHL}				1.0	—	4.6	ns
Setup Time	t_{su}	D	Q, $\overline{Q}$		—	—	2.5	ns
		A			—	—	3.5	
Hold Time	t_h	D	Q, $\overline{Q}$		—	—	1.5	ns
		A			—	—	1.0	
Rise/Fall Time	t_{TLH}	D	Q, $\overline{Q}$		1.5	—	3.5	ns
	t_{THL}				1.5	—	3.5	ns

■SWITCHING TIME TEST CIRCUIT





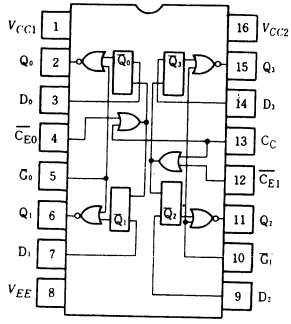
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.
4. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
5. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

HD10133

Quadruple Latches

The HD10133 is a high speed, low power quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock. The outputs are gated when the output enable($\overline{G}$) is low. All four latches may be clocked at one time with the common clock(C_C), or each half may be clocked separately with its clock enable ($\overline{CE}$).

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

$\overline{G}$	C	D	Q_{n+1}
H	×	×	L
L	L	×	Q_n
L	H	L	L
L	H	H	H

Notes) × : Don't care.
$C = C_C + \overline{C}_E$

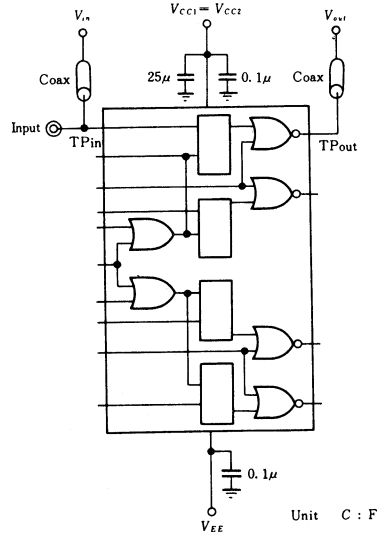
■DC CHARACTERISTICS ($V_{EE} = -5.2V$, $Ta = -30 \sim +85°C$)

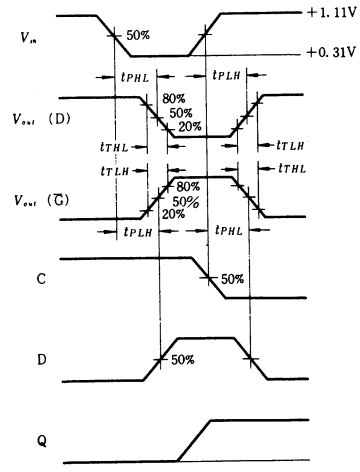
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	60	75	mA
Input Current	I_{IH}	$V_{IH} = -0.810V$	D	25℃	—	—	245	μA
			$\overline{C}_E$		—	—	265	
			$\overline{G}$, C_C		—	—	350	
	I_{IL}	$V_{IL} = -1.850V$		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH} = -0.890V$ or $V_{IL} = -1.890V$		−30℃	−1.060	—	−0.890	V
		$V_{IH} = -0.810V$ or $V_{IL} = -1.850V$		25℃	−0.960	—	−0.810	
		$V_{IH} = -0.700V$ or $V_{IL} = -1.825V$		85℃	−0.890	—	−0.700	
	V_{OL}	$V_{IL} = -1.890V$ or $V_{IH} = -0.890V$		−30℃	−1.890	—	−1.675	V
		$V_{IL} = -1.850V$ or $V_{IH} = -0.810V$		25℃	−1.850	—	−1.650	
		$V_{IL} = -1.825V$ or $V_{IH} = -0.700V$		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA} = -1.205V$ or $V_{ILA} = -1.500V$		−30℃	−1.080	—	—	V
		$V_{IHA} = -1.105V$ or $V_{ILA} = -1.475V$		25℃	−0.980	—	—	
		$V_{IHA} = -1.035V$ or $V_{ILA} = -1.440V$		85℃	−0.910	—	—	
	V_{OLA}	$V_{ILA} = -1.500V$ or $V_{IHA} = -1.205V$		−30℃	—	—	−1.655	V
		$V_{ILA} = -1.475V$ or $V_{IHA} = -1.105V$		25℃	—	—	−1.630	
		$V_{ILA} = -1.440V$ or $V_{IHA} = -1.035V$		85℃	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	D	Q	R_L = 50Ω	−30°C	1.0	—	5.6	ns
					25°C	1.0	—	5.4	
					85°C	1.1	—	5.9	
	t_{PHL}				−30°C	1.0	—	5.6	ns
					25°C	1.0	—	5.4	
					85°C	1.1	—	5.9	
	t_{PLH}	$\overline{C_E}$	Q		−30°C	1.0	—	5.4	ns
					25°C	1.0	—	5.4	
					85°C	1.2	—	6.0	
	t_{PHL}				−30°C	1.0	—	5.4	ns
					25°C	1.0	—	5.4	
					85°C	1.2	—	6.0	
	t_{PLH}	$\overline{G}$	Q		−30°C	1.0	—	3.2	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.4	
	t_{PHL}				−30°C	1.0	—	3.2	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.4	
Rise/Fall Time	t_{TLH}	D	Q		−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.8	
	t_{THL}				−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.8	
Setup Time	t_{su}	D	Q		25°C	—	—	2.5	ns
Hold Time	t_h				25°C	—	—	1.5	ns

■SWITCHING TIME TEST CIRCUIT





Notes)

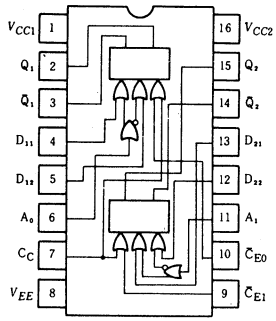
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.
4. t_{su} is the minimum time before the positive transition of the clock pulse that information must be preset at the data.
5. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

Dual Multiplexers with Latch

The HD10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock(C_C).

The data select inputs determine which data input is enabled. A high(H) level on the A0 input enables data input D12 and a low(L) level on the A0 input enables data input D11. A high(H) level on the A1 input enables data input D22 and a low(L) level on the A1 input enables data input D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

C	A_0	D_{11}	D_{12}	Q_{n+1}
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H
H	×	×	×	Q_n

Notes) × : Don't care.
$C=\overline{C}_E+C_C$

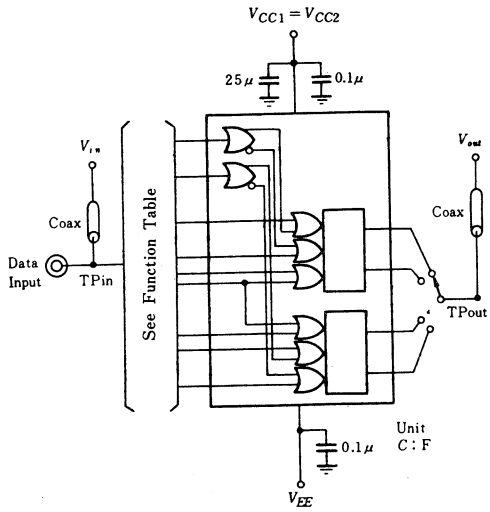
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

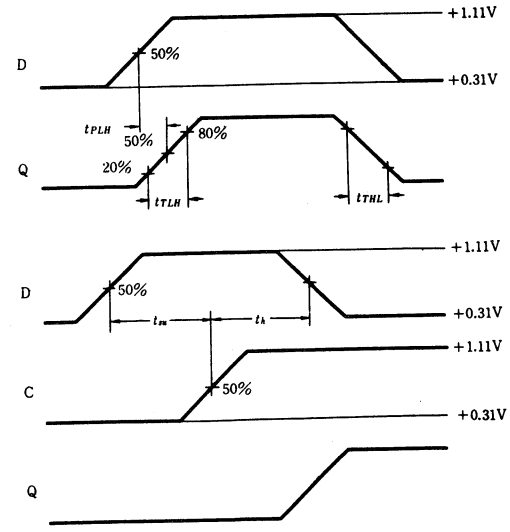
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	—	55	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	D, C_C	25℃	—	—	290	μA
			A, $\overline{C_E}$		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30℃	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25℃	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85℃	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30℃	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25℃	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30℃	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25℃	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85℃	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30℃	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25℃	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85℃	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE}=−3.2V, V_{CC}=+2.0V, Ta=25°C)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	D	Q, $\overline{Q}$	R_L=50Ω	1.0	—	3.3	ns
	t_{PHL}				1.0	—	3.3	ns
	t_{PLH}	$\overline{C_E}$	Q, $\overline{Q}$		1.0	—	5.7	ns
	t_{PHL}				1.0	—	5.7	ns
	t_{PLH}	A	Q, $\overline{Q}$		1.0	—	4.6	ns
	t_{PHL}				1.0	—	4.6	ns
Setup Time	t_{su}	D	Q, $\overline{Q}$		—	—	2.5	ns
		A	Q, $\overline{Q}$		—	—	3.5	
Hold Time	t_h	D	Q, $\overline{Q}$		—	—	1.5	ns
		A	Q, $\overline{Q}$		—	—	1.0	
Rise/Fall Time	t_{TLH}	D	Q, $\overline{Q}$		1.5	—	3.5	ns
	t_{THL}				1.5	—	3.5	ns

■SWITCHING TIME TEST CIRCUIT





Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.
4. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
5. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

HD10136

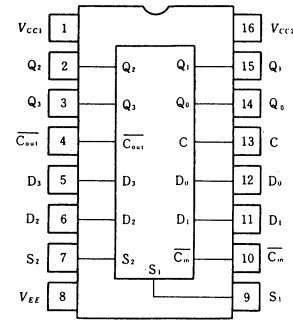
Universal Hexadecimal Counter

The HD10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous counter feature makes the HD10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs(D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

■PIN ARRANGEMENT



(Top View)

■FUNCTION SELECT TABLE

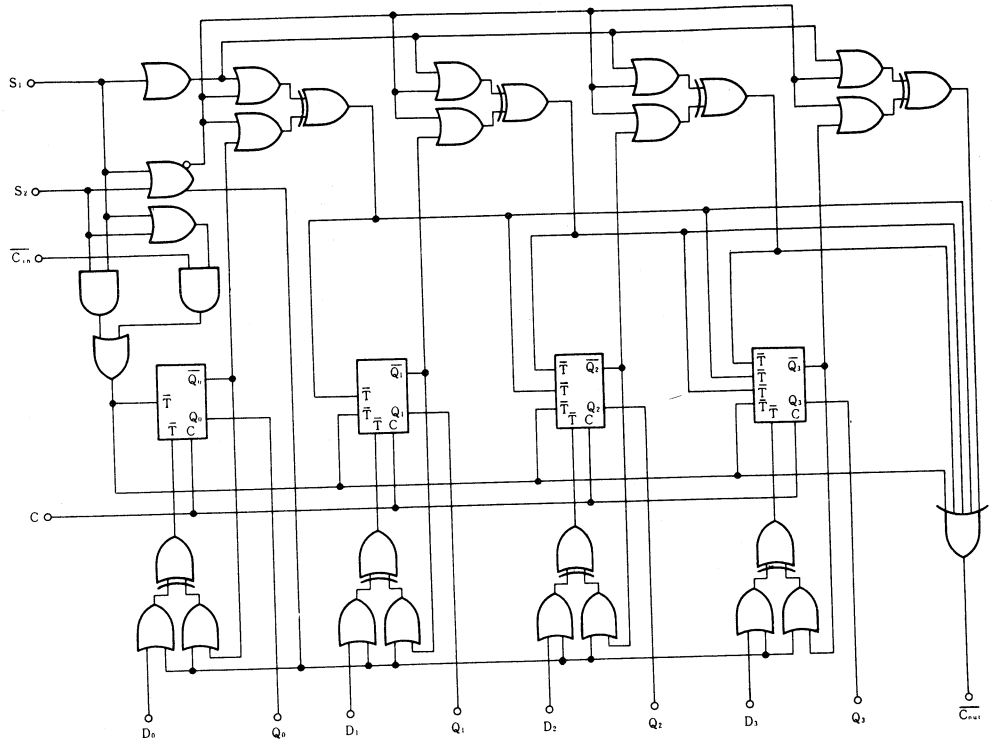
S_1	S_2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

■TRUTH TABLE

Inputs								Outputs				
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{Cin}$	C	Q_0	Q_1	Q_2	Q_3	$\overline{Cout}$
L	L	L	L	H	H	×	↑	L	L	H	H	L
L	H	×	×	×	×	L	↑	H	L	H	H	H
L	H	×	×	×	×	L	↑	L	H	H	H	H
L	H	×	×	×	×	L	↑	H	H	H	H	L
L	H	×	×	×	×	H	L	H	H	H	H	H
L	H	×	×	×	×	H	↑	H	H	H	H	H
H	H	×	×	×	×	×	↑	H	H	H	H	H
L	L	H	H	L	L	×	↑	H	H	L	L	L
H	L	×	×	×	×	L	↑	L	H	L	L	H
H	L	×	×	×	×	L	↑	H	L	L	L	H
H	L	×	×	×	×	L	↑	L	L	L	L	L
H	L	×	×	×	×	L	↑	H	H	H	H	H

Notes) 1. × : Don't care.
2. A ↑ is defined as a clock input transition from a low to a high logic level.

■BLOCK DIAGRAM



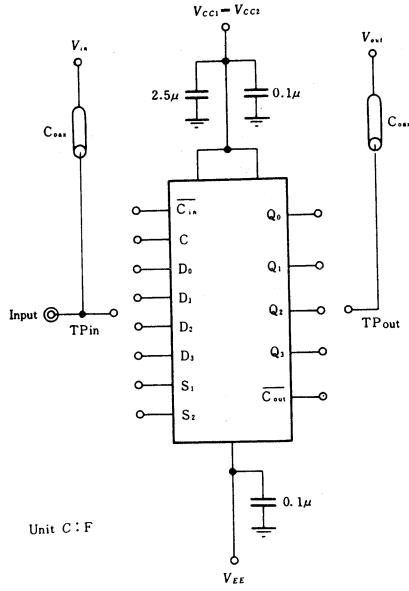
■DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

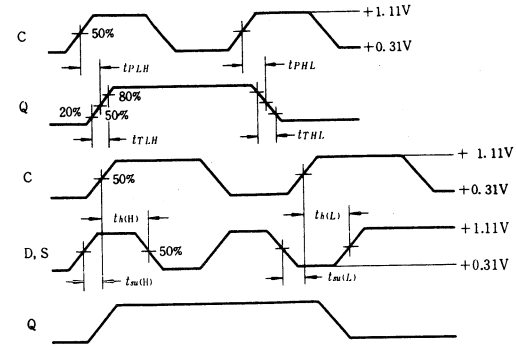
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	120	150	mA
Input Current	I_{IH}	V_{IH} = −0.810V	D	25°C	—	—	220	μA
			S_2		—	—	265	
			S_1, $\overline{Cin}$		—	—	245	
			C		—	—	290	
	I_{IL}	V_{IL} = −1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V		25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V		−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V		25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V		−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V		25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V		−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V		25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE}=−3.2V, V_{CC}=+2.0V, Ta=−30~+85℃)

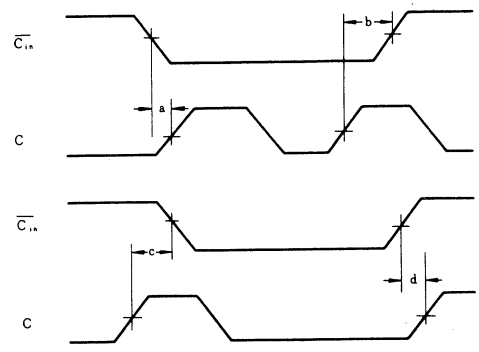
Item		Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time		t_{PLH}	C	Q	R_L=50Ω	−30℃	0.8	—	4.8	ns
						25℃	1.0	3.3	4.5	
						85℃	1.4	—	5.0	
		t_{PHL}				−30℃	0.8	—	4.8	ns
						25℃	1.0	3.3	4.5	
						85℃	1.4	—	5.0	
		t_{PLH}	C	$\overline{Cout}$		−30℃	2.0	—	10.9	ns
						25℃	2.5	7.0	10.5	
						85℃	2.4	—	11.5	
		t_{PHL}				−30℃	2.0	—	10.9	ns
						25℃	2.5	7.0	10.5	
						85℃	2.4	—	11.5	
		t_{PLH}	$\overline{Cin}$	$\overline{Cout}$		−30℃	1.6	—	7.4	ns
						25℃	1.6	5.0	6.9	
						85℃	1.9	—	7.5	
		t_{PHL}				−30℃	1.6	—	7.4	ns
						25℃	1.6	5.0	6.9	
						85℃	1.9	—	7.5	
Setup Time		$t_{su(H)}$	D, C	Q		25℃	—	—	3.5	ns
		$t_{su(L)}$					—	—	3.5	ns
		t_{su}	S_1, C	Q			—	—	7.5	ns
			S_2, C	Q			—	—	7.5	
			$\overline{Cin}$, C	Q			—	—	3.7	
			C, $\overline{Cin}$	Q			—	—	−1.0	
Hold Time		$t_{h(H)}$	C, D	Q		25℃	—	—	−0.3	ns
		$t_{h(L)}$					—	—	−0.3	ns
		t_h	C, S_1	Q			—	—	−2.5	ns
			C, S_2	Q			—	—	−2.5	
			C, $\overline{Cin}$	Q			—	—	−1.6	
			$\overline{Cin}$, C	Q			—	—	3.1	
Count Frequency	Count Up	f_{count}	C	Q		−30℃	125	—	—	MHz
						25℃	125	150	—	
						85℃	125	—	—	
	Count Down					−30℃	125	—	—	
						25℃	125	150	—	
						85℃	125	—	—	
Rise Time		t_{TLH}	C	$\overline{Cout}$		−30℃	0.9	—	3.3	ns
						25℃	1.1	2.0	3.3	
						85℃	1.1	—	3.5	
			C	Q		−30℃	0.9	—	3.3	
						25℃	1.1	2.0	3.3	
						85℃	1.1	—	3.5	
Fall Time		t_{THL}	C	$\overline{Cout}$		−30℃	0.9	—	3.3	ns
						25℃	1.1	2.0	3.3	
						85℃	1.1	—	3.5	
			C	Q		−30℃	0.9	—	3.3	
						25℃	1.1	2.0	3.3	
						85℃	1.1	—	3.5	

■SWITCHING TIME TEST CIRCUIT





Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.
4. t_{su} is the minimum time before the positive transition of the clock pulse that information must present at the data.
5. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

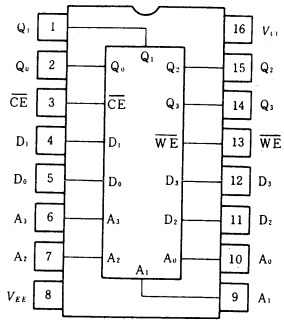


Notes)
1. (a) is the minimum time to wait after the count has been enabled to clock it.
2. (b) is the minimum time before the counter has been disabled that it may be clocked.
3. (c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.
4. (d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.
5. (b) and (c) may be negative numbers.

64-bit Register File

The HD10145 is a 16 word x 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 through A3. The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance. The operating mode of the RAM($\overline{CE}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode- the output is low and the data present at Dn is stored at the selected address.
With $\overline{WE}$ high the chip is in the read mode- The data state at the selected memory location is presented non-inverted at Qn.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

Mode	Inputs			Output
	$\overline{CE}$	$\overline{WE}$	D	Q
Write "L"	L	L	L	L
Write "H"	L	L	H	L
Read	L	H	×	Q
Disabled	H	×	×	L

Note) × : Don't care.

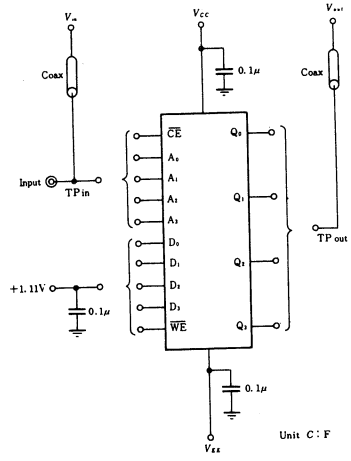
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85℃$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	120	150	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	$\overline{CE}$, A	25℃	—	—	200	μA
			D		—	—	220	
			$\overline{WE}$		—	—	470	
	I_{IL}	$V_{IL}=-1.850V$		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30℃	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25℃	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85℃	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30℃	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25℃	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30℃	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25℃	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85℃	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30℃	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25℃	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85℃	—	—	−1.595	

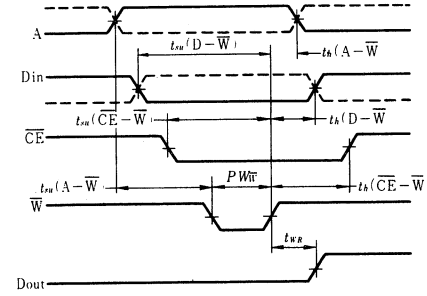
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=25°C$)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Access Time	t_A	$\overline{CE}$	Q	$R_L=50\Omega$	—	7.0	10	ns
		A	Q		—	10	15	
Setup Time	t_{su}	D→$\overline{W}$	Q		—	7.5	11	ns
		$\overline{CE}$→$\overline{W}$	Q		—	11	16	
		A→$\overline{W}$	Q		—	3.5	6	
Hold Time	t_h	D→$\overline{W}$	Q		—	3.0	5	ns
		$\overline{CE}$→$\overline{W}$	Q		—	3.0	5	
		A→$\overline{W}$	Q		—	3.5	5	
Write Recovery Time	t_{WR}	$\overline{W}$	Q		—	7.5	11	ns
Write Pulse Width	$PW_{\overline{W}}$	$\overline{W}$			—	7.5	15	ns
Setup Time	t_{su}	D→$\overline{CE}$	Q		—	7.5	11	ns
		$\overline{W}$→$\overline{CE}$	Q		—	11	16	
		A→$\overline{CE}$	Q		—	3.0	5	
Hold Time	t_h	D→$\overline{CE}$	Q		—	3.0	5	ns
		$\overline{W}$→$\overline{CE}$	Q		—	3.0	5	
		A→$\overline{CE}$	Q		—	3.0	5	
Chip Enable Pulse Width	$PW_{\overline{CE}}$	$\overline{CE}$			—	7.5	11	ns
Rise/Fall Time	t_{TLH}		Q		—	3.0	3.3	ns
	t_{THL}				—	3.0	3.3	ns

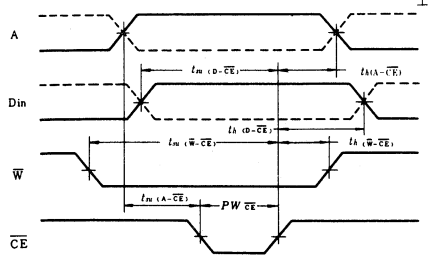
■SWITCHING TIME TEST CIRCUIT



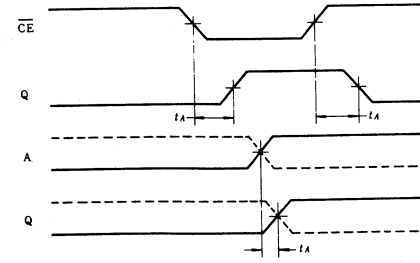
1. Write Timing-Write Strobe Mode



2. Chip Enable Strobe Mode



3. Read Timing

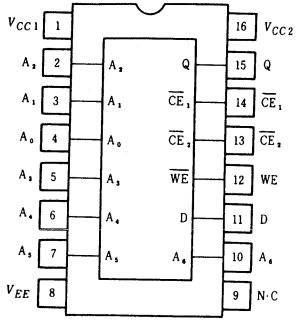


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

128-word×1-bit Random Access Memory

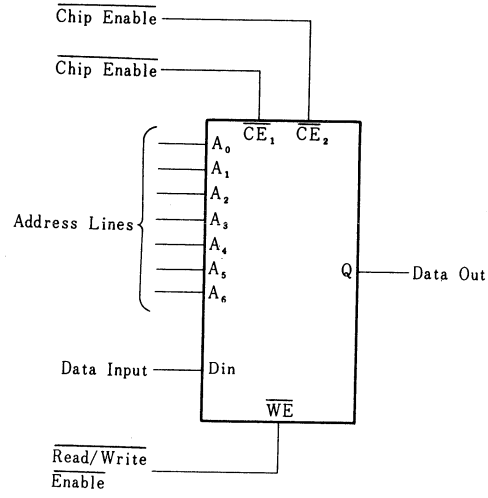
The HD10147 is a fast 128-word x 1-bit RAM. Bit selection is achieved by means of a 7-bit address, A0 through A6. The active-low chip selects and fast chip select access time allow easy memory expansion up to 512 words without affecting system performance. The operating mode ($\overline{CE}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode- the output is low and the data present at Dn is stroed at the selected address. With $\overline{WE}$ high the chip is in the read mode- the data state at the selected memory location is presented non-inverted at Dout.

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■FUNCTION TABLE

Mode	Input				Output
	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	Din	Dout
Write "L"	L	L	L	L	L
Write "H"	L	L	L	H	L
Read	L	L	H	×	Q
Disabled	H	L	×	×	L
	L	H	×	×	L

Note) × : Don't care.

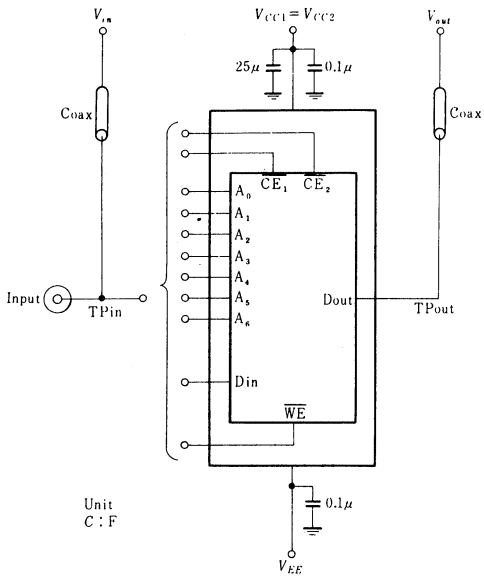
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85℃$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	80	100	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	A, D, $\overline{CE}$	25℃	—	—	35	μA
			$\overline{WE}$		—	—	75	
	I_{IL}	$V_{IL}=-1.850V$	A, $\overline{WE}$	25℃	−6.0	—	6.0	μA
			D, $\overline{CE}$		—	—	6.0	
Output Voltage	V_{OH}	$\overline{WE}=-1.205V$, $\overline{CE}=-1.500V$		−30℃	−1.060	—	−0.890	V
		$\overline{WE}=-1.105V$, $\overline{CE}=-1.475V$		25℃	−0.960	—	−0.810	
		$\overline{WE}=-1.035V$, $\overline{CE}=-1.440V$		85℃	−0.890	—	−0.700	
	V_{OL}	$\overline{WE}=-1.205V$, $\overline{CE}=-1.500V$		−30℃	−1.890	—	−1.675	V
		$\overline{WE}=-1.105V$, $\overline{CE}=-1.475V$		25℃	−1.850	—	−1.650	
		$\overline{WE}=-1.035V$, $\overline{CE}=-1.440V$		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$\overline{WE}=-1.205V$, $\overline{CE}=-1.500V$		−30℃	−1.080	—	—	V
		$\overline{WE}=-1.105V$, $\overline{CE}=-1.475V$		25℃	−0.980	—	—	
		$\overline{WE}=-1.035V$, $\overline{CE}=-1.440V$		85℃	−0.910	—	—	
	V_{OLA}	$\overline{CE_1}$ or $\overline{CE_2}=-1.205V$		−30℃	—	—	−1.655	V
		$\overline{CE_1}$ or $\overline{CE_2}=-1.105V$		25℃	—	—	−1.630	
		$\overline{CE_1}$ or $\overline{CE_2}=-1.035V$		85℃	—	—	−1.595	

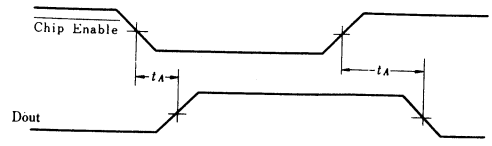
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=25℃$)

Item		Symbol	Input	Output	Test Condition	min	typ	max	Unit
Access Time		t_A	$\overline{CE}$	Q	$R_L=50Ω$	—	—	8.0	ns
			A_5	Q		—	10	12	
			A_0	Q		—	9	10	
Write Strobe Mode	Setup Time	t_{su}	D→$\overline{WE}$	Q		1.0	—	—	ns
			$\overline{CE}$→$\overline{WE}$	Q		1.0	—	—	
			A_2→$\overline{WE}$	Q		3.0	—	—	
			A_5→$\overline{WE}$	Q		4.0	—	—	
	Hold Time	t_h	D→$\overline{WE}$	Q		1.0	—	—	ns
			$\overline{CE}$→$\overline{WE}$	Q		1.0	—	—	
			A→$\overline{WE}$	Q		3.0	—	—	
Write Recovery Time		t_{WR}	$\overline{WE}$	Q		—	—	8.0	ns
Write Pulse Width		$t_{W(\overline{WE})}$	$\overline{WE}$	Q		—	—	8.0	ns
Rise Time		t_{TLH}		Q		—	2.0	—	ns
Fall Time		t_{THL}				—	1.0	—	ns

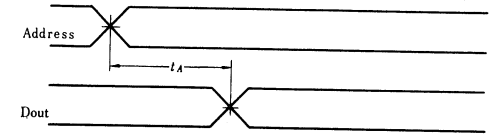
■SWITCHING TIME TEST CIRCUIT



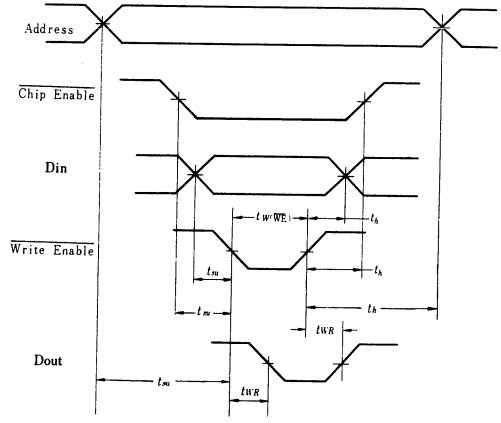
1. Chip Enable Access Time



2. Address Access Time



3. Write Strobe Mode



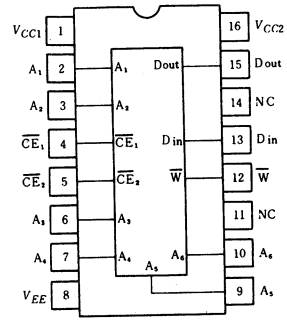
Notes) 1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

HD10148

64-bit Random Access Memory

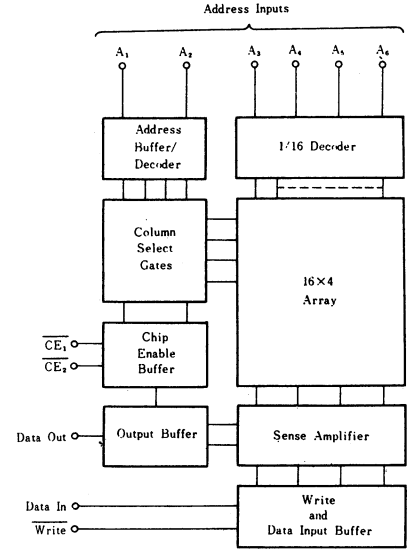
The HD10148 is a fast 64-word x 1-bit RAM. Bit selection is achieved by means of a 6-bit address, A0 through A5. The active low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance. The operating mode ($\overline{CE}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode- The output is low and the data present at Din is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode- the data state at the selected memory location is presented non-inverted at Dout.

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■FUNCTION TABLE

Mode	Inputs			Output
	$\overline{CE}$	$\overline{WE}$	Din	Dout
Write "L"	L	L	L	L
Write "H"	L	L	H	L
Read	L	H	×	Q
Disabled	H	×	×	L

× : Don't care.
$\overline{CE}=\overline{CE_1}+\overline{CE_2}$

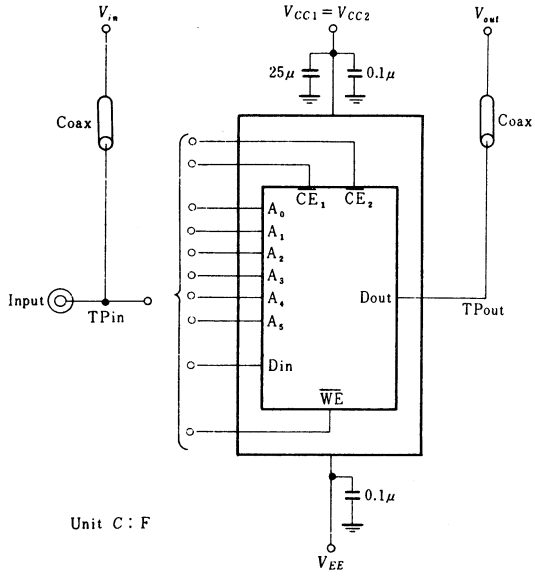
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	80	130	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	A	25°C	—	—	265	μA
			$\overline{CE}$		—	—	50	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$		85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

Item		Symbol	Input	Output	Test Condition	min	typ	max	Unit
Access Time		t_A	$\overline{CE}$	Dout	R_L = 50Ω	—	—	12	ns
			A	Dout		—	—	15	
Pulse Width		t_w	$\overline{WE}$	Dout		—	—	10	ns
			$\overline{CE}$	Dout		—	—	13	
Write Strobe Mode	Setup Time	t_{su}	Din→$\overline{WE}$	Dout		—	—	0	ns
			$\overline{CE}$→$\overline{WE}$	Dout		—	—	3	
			A→$\overline{WE}$	Dout		—	—	5	
	Hold Time	t_h	$\overline{WE}$→Din	Dout		—	—	3	ns
			$\overline{WE}$→$\overline{CE}$	Dout		—	—	0	
			$\overline{WE}$→A	Dout		—	—	3	

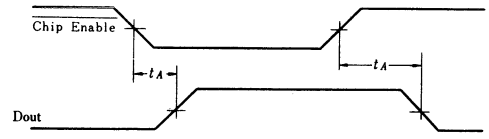
■ SWITCHING TIME TEST CIRCUIT



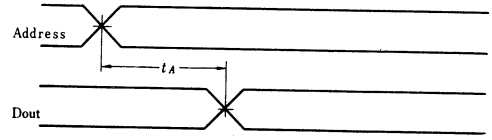
Unit C : F

Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

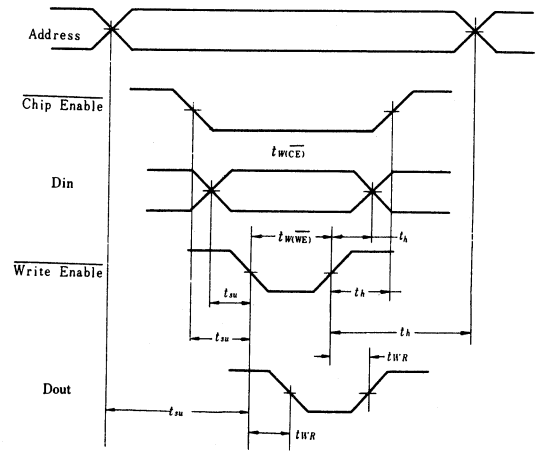
1. Chip Enable Access Time



2. Address Access Time



3. Write Strobe Mode



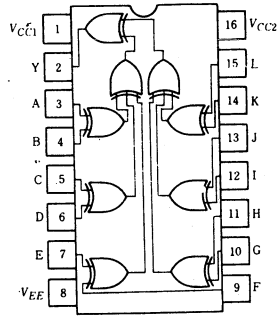
HD10160

12-bit Parity Generator/Checker

The HD10160 consists of nine Exclusive-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high.

Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

Inputs	Output
Sum of High Level Inputs	Y
Even	H
Odd	L

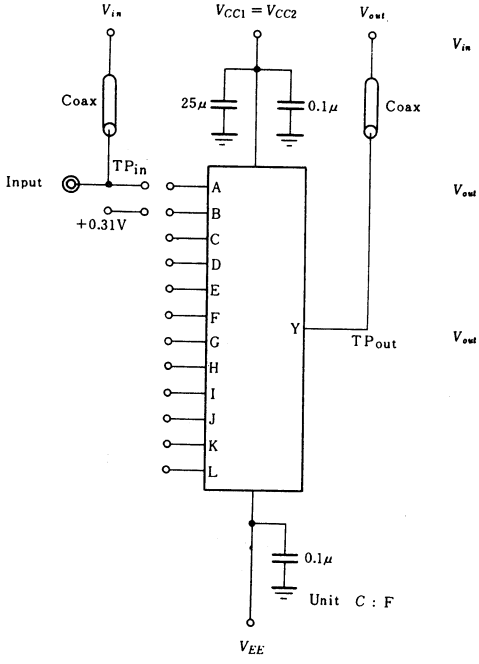
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85℃$)

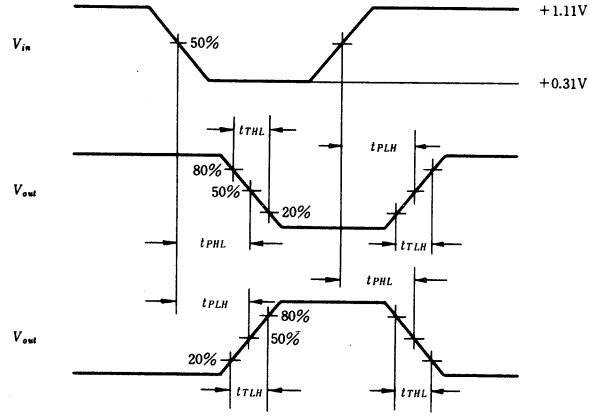
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	B, C, F, G, J, K = −0.810V		25℃	—	62	78	mA
Input Current	I_{IH}	V_{IH} = −0.810V	A, D, E, H, I, L	25℃	—	—	265	μA
			B, C, F, G, J, K		—	—	220	
	I_{IL}	V_{IL} = −1.850V		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	Each one input = −0.890V, Other inputs = −1.890V		−30℃	−1.060	—	−0.890	V
		Each one input = −0.810V, Other inputs = −1.850V		25℃	−0.960	—	−0.810	
		Each one input = −0.700V, Other inputs = −1.825V		85℃	−0.890	—	−0.700	
	V_{OL}	All inputs = −1.890V		−30℃	−1.890	—	−1.675	V
		All inputs = −1.850V		25℃	−1.850	—	−1.650	
		All inputs = −1.825V		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	Each one input = −1.205V, Other inputs = −1.890V		−30℃	−1.080	—	—	V
		Each one input = −1.105V, Other inputs = −1.850V		25℃	−0.980	—	—	
		Each one input = −1.035V, Other inputs = −1.825V		85℃	−0.910	—	—	
	V_{OLA}	Each one input = −1.500V, Other inputs = −1.890V		−30℃	—	—	−1.655	V
		Each one input = −1.475V, Other inputs = −1.850V		25℃	—	—	−1.630	
		Each one input = −1.440V, Other inputs = −1.825V		85℃	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30~+85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L=50Ω	−30℃	1.8	—	8.1	ns
			25℃	2.0	5.0	7.5	
			85℃	2.0	—	8.0	
	t_{PHL}		−30℃	1.8	—	8.1	ns
			25℃	2.0	5.0	7.5	
			85℃	2.0	—	8.0	
Rise/Fall Time	t_{TLH}		−30℃	1.1	—	3.5	ns
			25℃	1.1	2.0	3.3	
			85℃	1.0	—	3.5	
	t_{THL}		−30℃	1.1	—	3.5	ns
			25℃	1.1	2.0	3.3	
			85℃	1.0	—	3.5	

■ SWITCHING TIME TEST CIRCUIT





Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

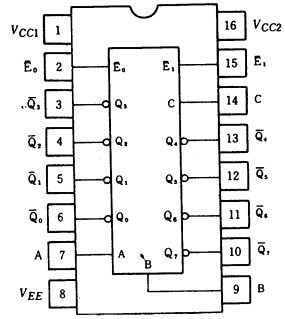
HD10161

Binary to 1-8 Decoder (low)

The HD10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high. The HD10161 is a true parallel decoder.

No series gating is used internally, eliminating unequal delay time found in other decoders. This design provides the identical 4ns delay from any address or enable input to any output.

■PIN ARRANGEMENT



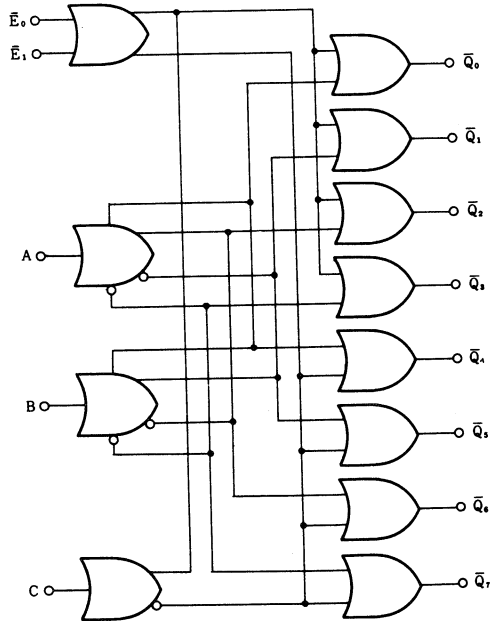
(Top View)

■FUNCTION TABLE

Enable Inputs		Inputs			Outputs							
$\overline{E}_1$	$\overline{E}_0$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	×	×	×	×	H	H	H	H	H	H	H	H
×	H	×	×	×	H	H	H	H	H	H	H	H

× : Don't Care

■BLOCK DIAGRAM



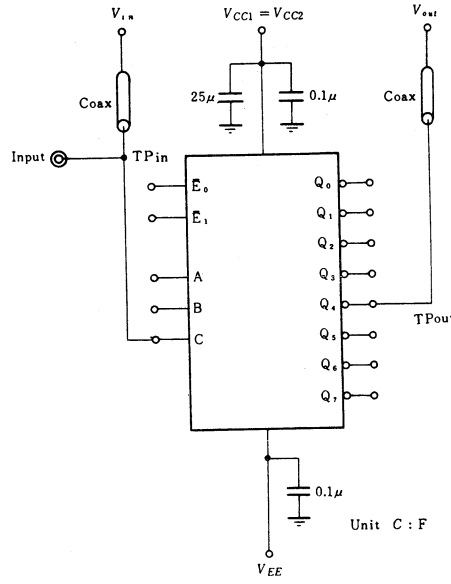
■ DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

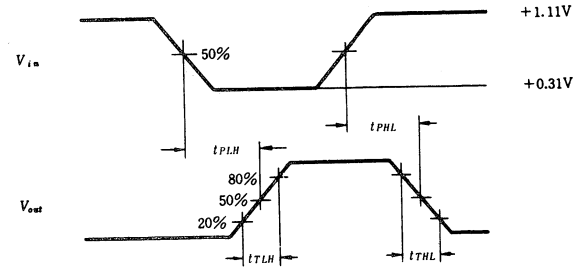
Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All inputs = −0.810V	25°C	—	61	76	mA
Input Current	I_{IH}	V_{IH} = −0.810V	25°C	—	—	220	μA
	I_{IL}	V_{IL} = −1.850V	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V	−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V	25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V	85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V	−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V	25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V	−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V	25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V	85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V	−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V	25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V	85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V , V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L = 50Ω	−30°C	1.5	—	6.2	ns
			25°C	1.5	4.0	6.0	
			85°C	1.5	—	6.4	
	t_{PHL}		−30°C	1.5	—	6.2	ns
			25°C	1.5	4.0	6.0	
			85°C	1.5	—	6.4	
Rise/Fall Time	t_{TLH}		−30°C	1.0	—	3.3	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.5	
	t_{THL}		−30°C	1.0	—	3.3	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.5	

■ SWITCHING TIME TEST CIRCUIT





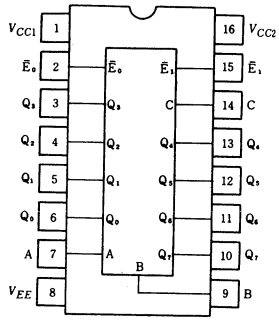
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

HD10162

Binary to 1-8 Decoder (high)

The HD10162 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low. The HD10162 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

■ PIN ARRANGEMENT



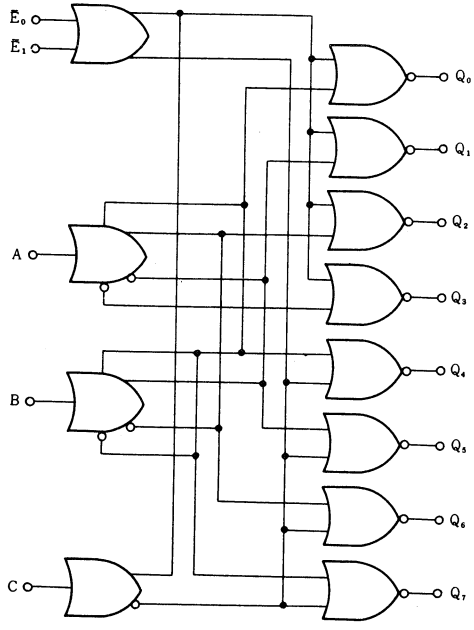
(Top View)

■ FUNCTION TABLE

Enable Inputs		Inputs			Outputs							
$\bar{E}_0$	$\bar{E}_1$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	×	×	×	×	L	L	L	L	L	L	L	L
×	H	×	×	×	L	L	L	L	L	L	L	L

× : Don't Care

■ BLOCK DIAGRAM



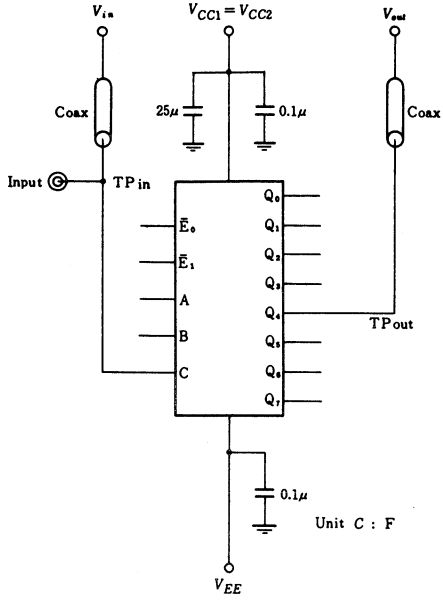
■ DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

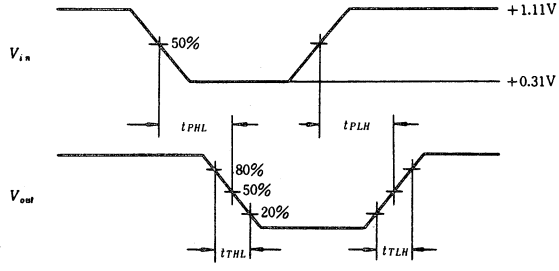
Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	61	76	mA
Input Current	I_{IH}	V_{IH} = −0.810V	25°C	—	—	220	μA
	I_{IL}	V_{IL} = −1.850V	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V	−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V	25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V	85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V	−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V	25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V	−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V	25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V	85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V	−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V	25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V	85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L = 50Ω	−30°C	1.5	—	6.2	ns
			25°C	1.5	4.0	6.0	
			85°C	1.5	—	6.4	
	t_{PHL}		−30°C	1.5	—	6.2	ns
			25°C	1.5	4.0	6.0	
			85°C	1.5	—	6.4	
Rise/Fall Time	t_{TLH}		−30°C	1.0	—	3.3	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.5	
	t_{THL}		−30°C	1.0	—	3.3	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.5	

■ SWITCHING TIME TEST CIRCUIT



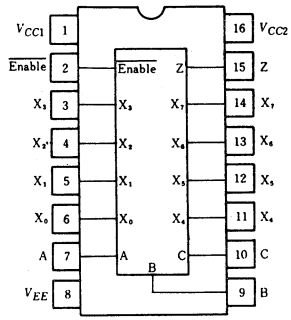


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

8 Line Multiplexer

The HD10164 can be used whenever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the HD10164 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The HD10164 can be connected directly to a data bus, due to its open emitter output and output enable.

■PIN ARRANGEMENT



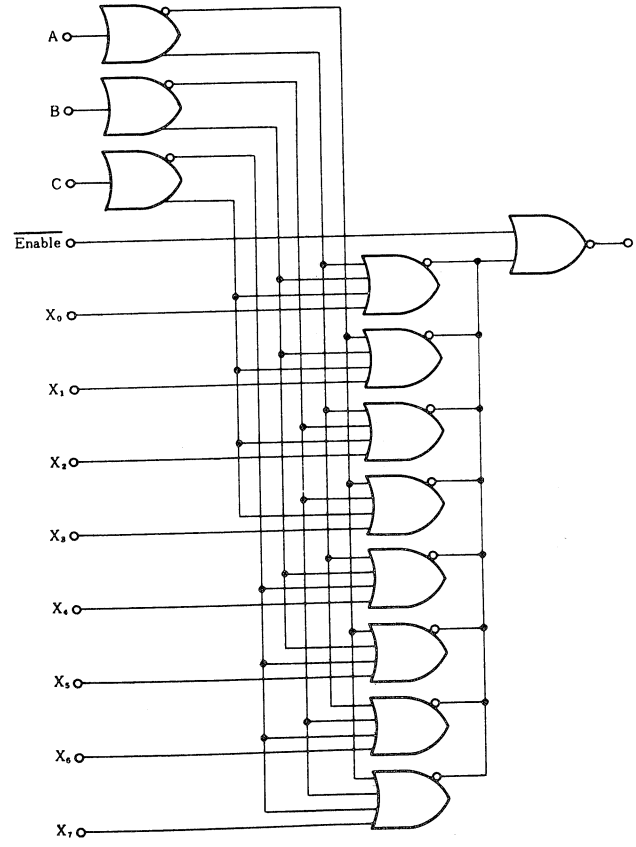
(Top View)

■FUNCTION TABLE

$\overline{Enable}$	Address Inputs			Z
	C	B	A	
L	L	L	L	X_0
L	L	L	H	X_1
L	L	H	L	X_2
L	L	H	H	X_3
L	H	L	L	X_4
L	H	L	H	X_5
L	H	H	L	X_6
L	H	H	H	X_7
H	×	×	×	L

× : Don't Care

■BLOCK DIAGRAM



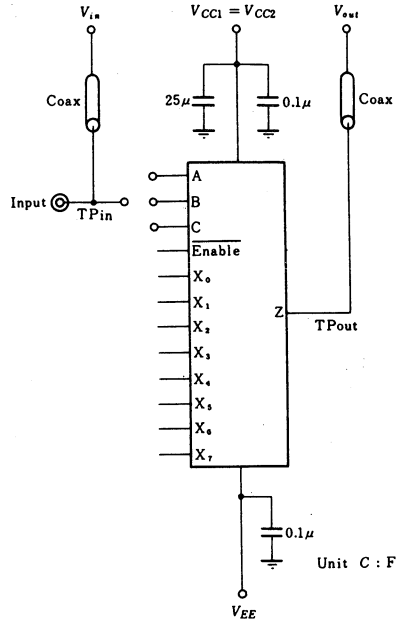
■ DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85℃)

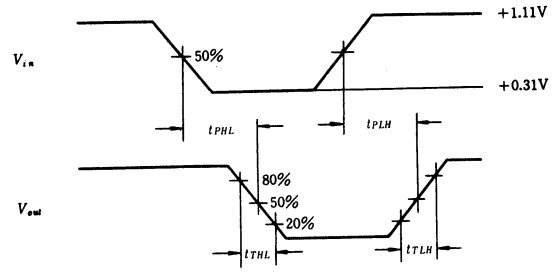
Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25℃	—	60	75	mA
Input Current	I_{IH}	V_{IH} = −0.810V	25℃	—	—	265	μA
	I_{IL}	V_{IL} = −1.850V	25℃	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V	−30℃	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V	25℃	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V	85℃	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V	−30℃	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V	25℃	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V	85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V	−30℃	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V	25℃	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V	85℃	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V	−30℃	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V	25℃	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V	85℃	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85℃)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	Address	Z	R_L = 50Ω	−30℃	1.5	—	4.7	ns
					25℃	1.5	3.0	4.5	
					85℃	1.6	—	4.8	
	t_{PHL}				−30℃	1.5	—	4.7	ns
					25℃	1.5	3.0	4.5	
					85℃	1.6	—	4.8	
	t_{PLH}	Data	Z		−30℃	1.9	—	6.3	ns
					25℃	2.0	4.0	6.0	
					85℃	2.2	—	6.5	
	t_{PHL}				−30℃	1.9	—	6.3	ns
					25℃	2.0	4.0	6.0	
					85℃	2.2	—	6.5	
	t_{PLH}	$\overline{\text{Enable}}$	Z		−30℃	0.9	—	3.3	ns
					25℃	1.0	2.0	2.9	
					85℃	1.0	—	3.1	
	t_{PHL}				−30℃	0.9	—	3.3	ns
					25℃	1.0	2.0	2.9	
					85℃	1.0	—	3.1	
Rise/Fall Time	t_{TLH}		Z		−30℃	0.9	—	3.3	ns
					25℃	1.1	2.0	3.3	
					85℃	1.2	—	3.6	
	t_{THL}				−30℃	0.9	—	3.3	ns
					25℃	1.1	2.0	3.3	
					85℃	1.2	—	3.6	

■ SWITCHING TIME TEST CIRCUIT

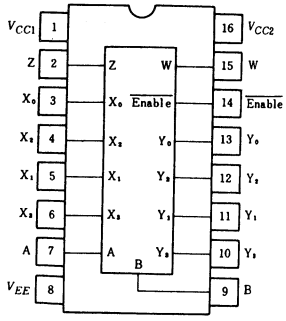




Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected in a 50Ω resistor to ground.

Dual 4 to 1 Multiplexers

■ PIN ARRANGEMENT



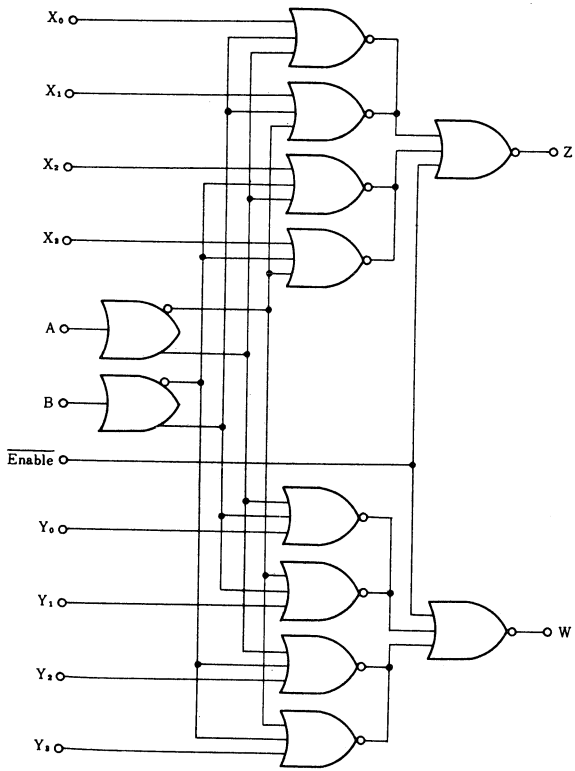
(Top View)

■ FUNCTION TABLE

Enable	Address Inputs		Outputs	
$\overline{E}$	B	A	Z	W
H	×	×	L	L
L	L	L	X_0	Y_0
L	L	H	X_1	Y_1
L	H	L	X_2	Y_2
L	H	H	X_3	Y_3

× : Don't Care

■ BLOCK DIAGRAM



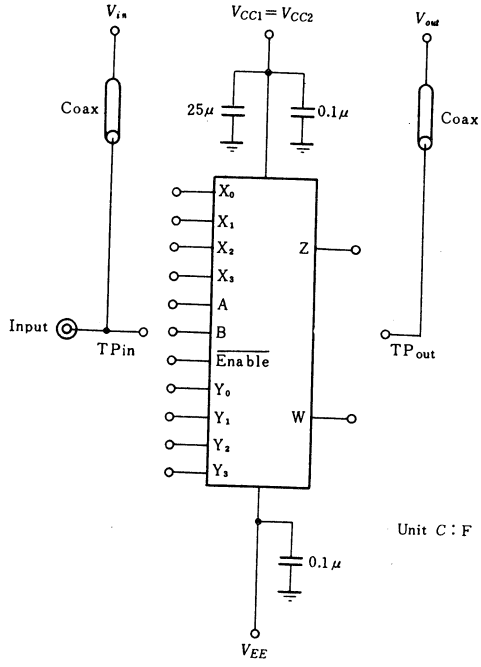
■ DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85℃)

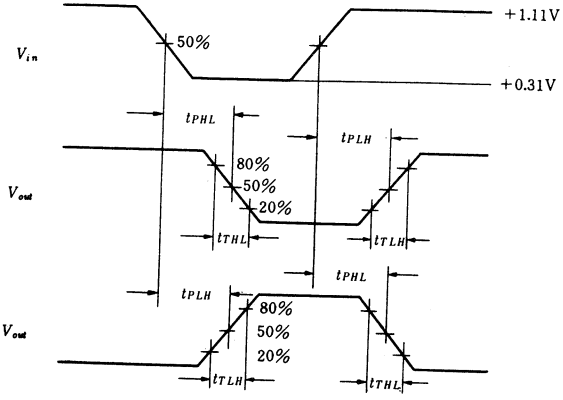
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	58	73	mA
Input Current	I_{IH}	V_{IH} = −0.810V	Data	25℃	—	—	220	μA
			Enable		—	—	330	
	I_{IL}	V_{IL} = −1.850V		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V		−30℃	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V		25℃	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V		85℃	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V		−30℃	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V		25℃	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V		−30℃	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V		25℃	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V		85℃	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V		−30℃	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V		25℃	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V		85℃	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85℃.)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	Data	Z, W	R_L=50Ω	−30℃	1.4	—	4.8	ns
					25℃	1.5	3.5	4.5	
					85℃	1.4	—	4.8	
	t_{PHL}				−30℃	1.4	—	4.8	ns
					25℃	1.5	3.5	4.5	
					85℃	1.4	—	4.8	
	t_{PLH}	Address	Z, W		−30℃	1.9	—	6.4	ns
					25℃	2.0	5.0	6.0	
					85℃	2.1	—	6.4	
	t_{PHL}				−30℃	1.9	—	6.4	ns
					25℃	2.0	5.0	6.0	
					85℃	2.1	—	6.4	
	t_{PLH}	Enable	Z, W		−30℃	1.0	—	3.1	ns
					25℃	1.0	2.0	2.9	
					85℃	0.9	—	3.2	
	t_{PHL}				−30℃	1.0	—	3.1	ns
					25℃	1.0	2.0	2.9	
					85℃	0.9	—	3.2	
Rise Time	t_{TLH}		Z, W		−30℃	1.0	—	3.4	ns
					25℃	1.1	2.0	3.3	
					85℃	1.1	—	3.6	
Fall Time	t_{THL}				−30℃	1.0	—	3.4	ns
					25℃	1.1	2.0	3.3	
					85℃	1.1	—	3.6	

■ SWITCHING TIME TEST CIRCUIT





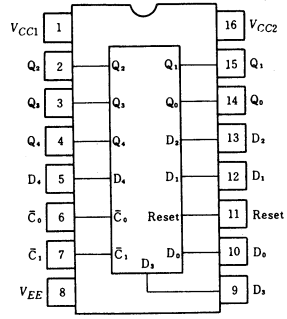
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

Quintuple Latches

The HD10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latches on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

■PIN ARRANGEMENT



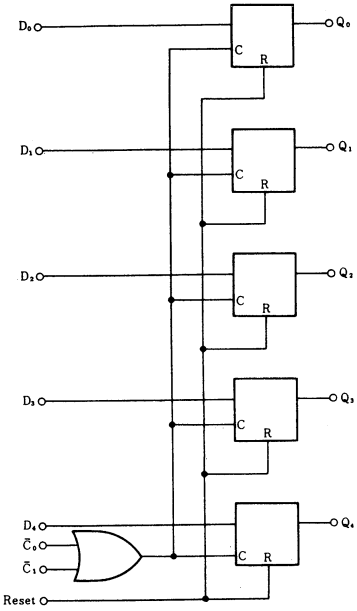
(Top View)

■FUNCTION TABLE

D	C_0	C_1	Reset	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
×	H	×	L	Q_n
×	×	H	L	Q_n
×	H	×	H	L
×	×	H	H	L

× : Don't Care

■BLOCK DIAGRAM



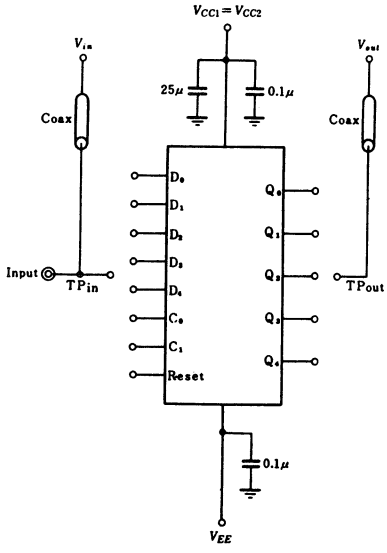
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	78	97	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	Clock, Data	25°C	—	—	290	μA
			Reset		—	—	650	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$, $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$, $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$, $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$, $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$, $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$, $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$		85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30~+85°C)

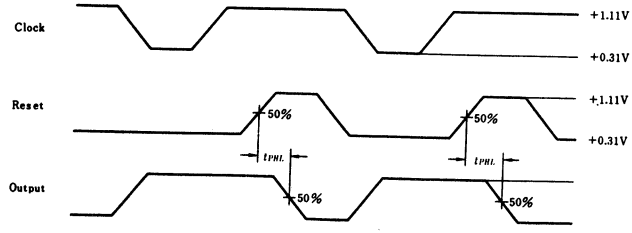
Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	Data	Q	R_L=50Ω	−30°C	1.0	—	3.6	ns
					25°C	1.0	—	3.5	
					85°C	1.0	—	3.6	
	t_{PHL}				−30°C	1.0	—	3.6	ns
					25°C	1.0	—	3.5	
					85°C	1.0	—	3.6	
	t_{PLH}	Clock	Q		−30°C	1.0	—	4.7	ns
					25°C	1.0	—	4.3	
					85°C	1.0	—	4.4	
	t_{PHL}				−30°C	1.0	—	4.7	ns
					25°C	1.0	—	4.3	
					85°C	1.0	—	4.4	
	t_{PHL}	Reset	Q		−30°C	0.9	—	4.0	ns
					25°C	1.0	—	3.9	
					85°C	1.0	—	4.2	
Setup Time	t_{su}	D→C	Q		25°C	—	—	2.5	ns
Hold Time	t_h				25°C	—	—	1.5	ns
Rise/Fall Time	t_{TLH}		Q		−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.7	
	t_{THL}				−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.7	

■ SWITCHING TIME TEST CIRCUIT

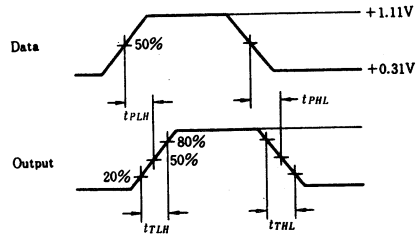


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

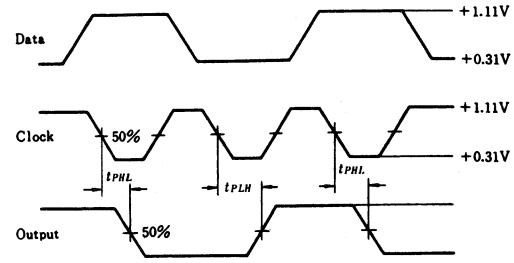
1. Reset



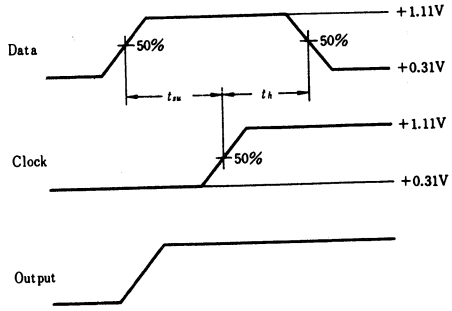
2. Data



3. Clock



4. Setup and Hold

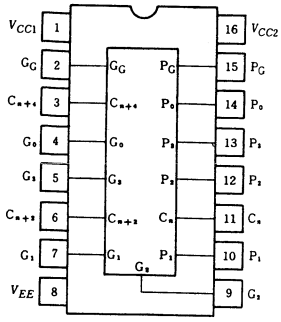


Notes) 1. t_{SU} is minimum time before the positive transition of the clock pulse that information must be present at the data.
2. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

Look-Ahead Carry Block

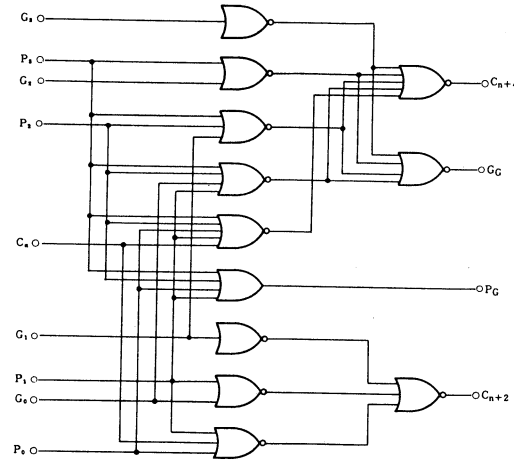
The HD10179 is a high speed, low power, standard ECL complex function that is designed to perform the look-ahead carry function. This device can be used with the HD10181 4-unit ALU directly, or with the HD10180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



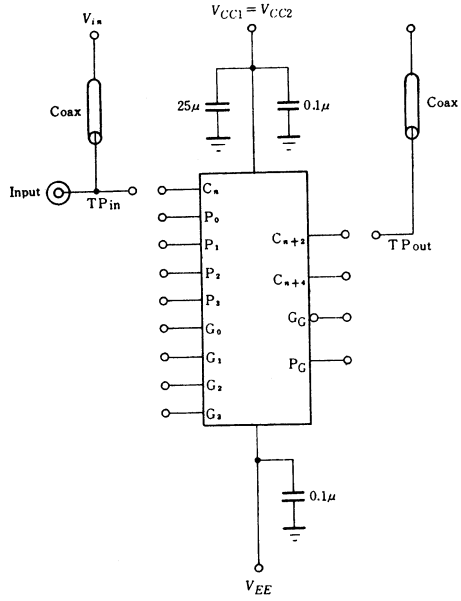
■ DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

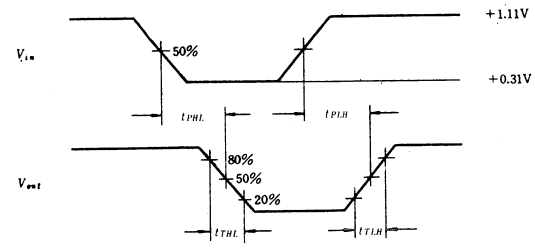
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	58	72	mA
Input Current	I_{IH}	V_{IH} = −0.810V	G_0, G_1, Cn	25°C	—	—	270	μA
			G_2, G_3		—	—	225	
			P_1, P_3		—	—	440	
			P_2		—	—	395	
			P_0		—	—	355	
	I_{IL}	V_{IL} = −1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V		25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V		−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V		25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V		−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V		25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V		−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V		25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	G_3	C_{n+4}	R_L = 50Ω	1.0	—	5.5	ns
	t_{PHL}				1.0	—	5.5	
	t_{PLH}	Cn	C_{n+2}		1.0	—	5.5	
	t_{PHL}				1.0	—	5.5	
	t_{PLH}	G_3	G_G		1.0	—	5.5	
	t_{PHL}				1.0	—	5.5	
	t_{PLH}	P_1	C_{n+Z}		1.0	—	5.5	
	t_{PHL}				1.0	—	5.5	
	t_{PLH}	P_1	P_G		1.0	—	3.5	
	t_{PHL}				1.0	—	3.5	
Rise Time	t_{TLH}	Cn	C_{n+Z}		1.1	—	3.5	ns
Fall Time	t_{THL}				1.1	—	3.5	ns

■SWITCHING TIME TEST CIRCUIT





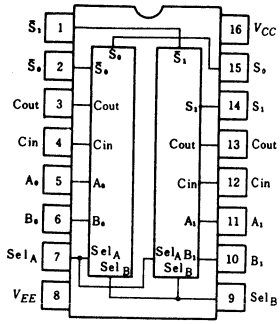
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

HD10180

Dual 2-bit Adders/Subtractors

The HD10180 is a high speed, low power, general-purpose adder/subtractor. Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, $\overline{\text{Sum}}$, and Carry-out. The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B.

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION SELECT TABLE

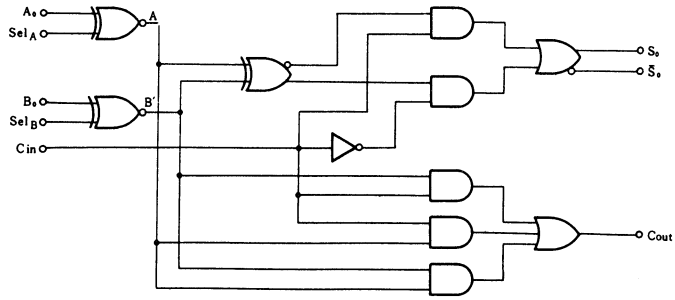
Sel_A	Sel_B	Function
H	H	S = A + B
H	L	S = A − B
L	H	S = B − A
L	L	S = 0 − A − B

■ FUNCTION TABLE

Function	Inputs					Outputs		
	Sel_A	Sel_B	A_0	B_0	Cin	S_0	$\overline{S_0}$	Cout
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H

Function	Inputs					Outputs		
	Sel_A	Sel_B	A_0	B_0	Cin	S_0	$\overline{S_0}$	Cout
REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	H
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	H
	L	L	H	L	L	H	L	L
	L	L	H	L	H	L	H	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

■ BLOCK DIAGRAM



HITACHI

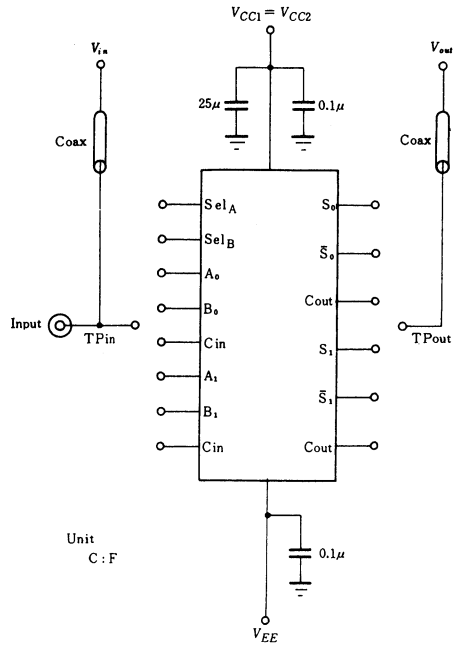
■DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30~+85°C)

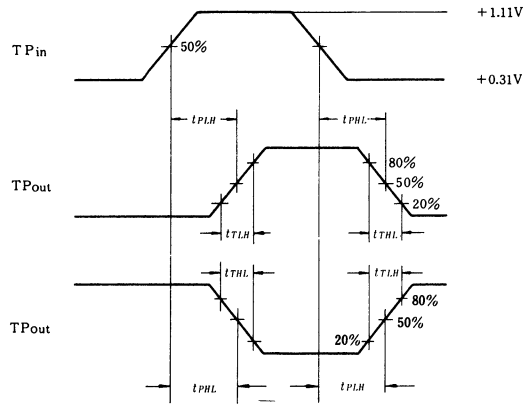
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	70	86	mA
Input Current	I_{IH}	V_{IH} = −0.810V	Cin	25°C	—	—	370	μA
			A, B		—	—	220	
			Sel_A, Sel_B		—	—	290	
	I_{IL}	V_{IL} = −1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V		25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V		−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V		25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V		−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V		25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V		−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V		25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30~+85°C)

Item		Symbol	Input	Output	Test Condition		min	typ	max.	Unit
Propagation Delay Time	Operand	t_{PLH} t_{PHL}	A_0	S_0	R_L=50Ω	−30°C	1.3	—	5.8	ns
						25°C	1.3	—	5.4	
						85°C	1.1	—	5.8	
			B_0	S_0		−30°C	1.3	—	5.8	
						25°C	1.3	—	5.4	
						85°C	1.1	—	5.8	
	Cin		Cin	S_0		−30°C	1.0	—	3.4	
						25°C	1.0	—	3.3	
						85°C	0.9	—	3.6	
			Cin	Cout		−30°C	1.0	—	3.4	
						25°C	1.0	—	3.3	
						85°C	0.9	—	3.6	
	Select		Sel_A	S_0		−30°C	1.3	—	5.8	
						25°C	1.3	—	5.4	
						85°C	1.1	—	5.8	
			Sel_B	S_0		−30°C	1.3	—	5.8	
						25°C	1.3	—	5.4	
						85°C	1.1	—	5.8	
Rise Time		t_{TLH}	A_0	S_0		−30°C	1.0	—	3.8	ns
						25°C	1.1	—	3.7	
						85°C	1.1	—	3.9	
Fall Time		t_{THL}				−30°C	1.0	—	3.8	ns
						25°C	1.1	—	3.7	
						85°C	1.1	—	3.9	

■ SWITCHING TIME TEST CIRCUIT





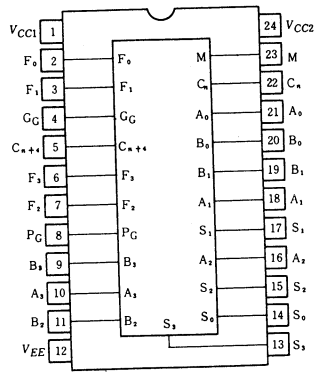
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

HD10181

4-bit Arithmetic Logic Unit/Function Generator

The HD10181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S1 through S3) as indicated in the table of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

■ PIN ARRANGEMENT



(Top View)

■ FUNCTIONS OF PIN NUMBER

Pin No.	Function
A_3, A_2, A_1, A_0	Word A Inputs
B_3, B_2, B_1, B_0	Word B Inputs
S_3, S_2, S_1, S_0	Function-Select Inputs
C_n	Ripple-Carry Input
M	Mode Control Input
F_3, F_2, F_1, F_0	Function Outputs
P_G	Carry Propagate Output
C_{n+4}	Ripple-Carry Output
G_G	Carry-Generate Output

■ FUNCTION TABLE

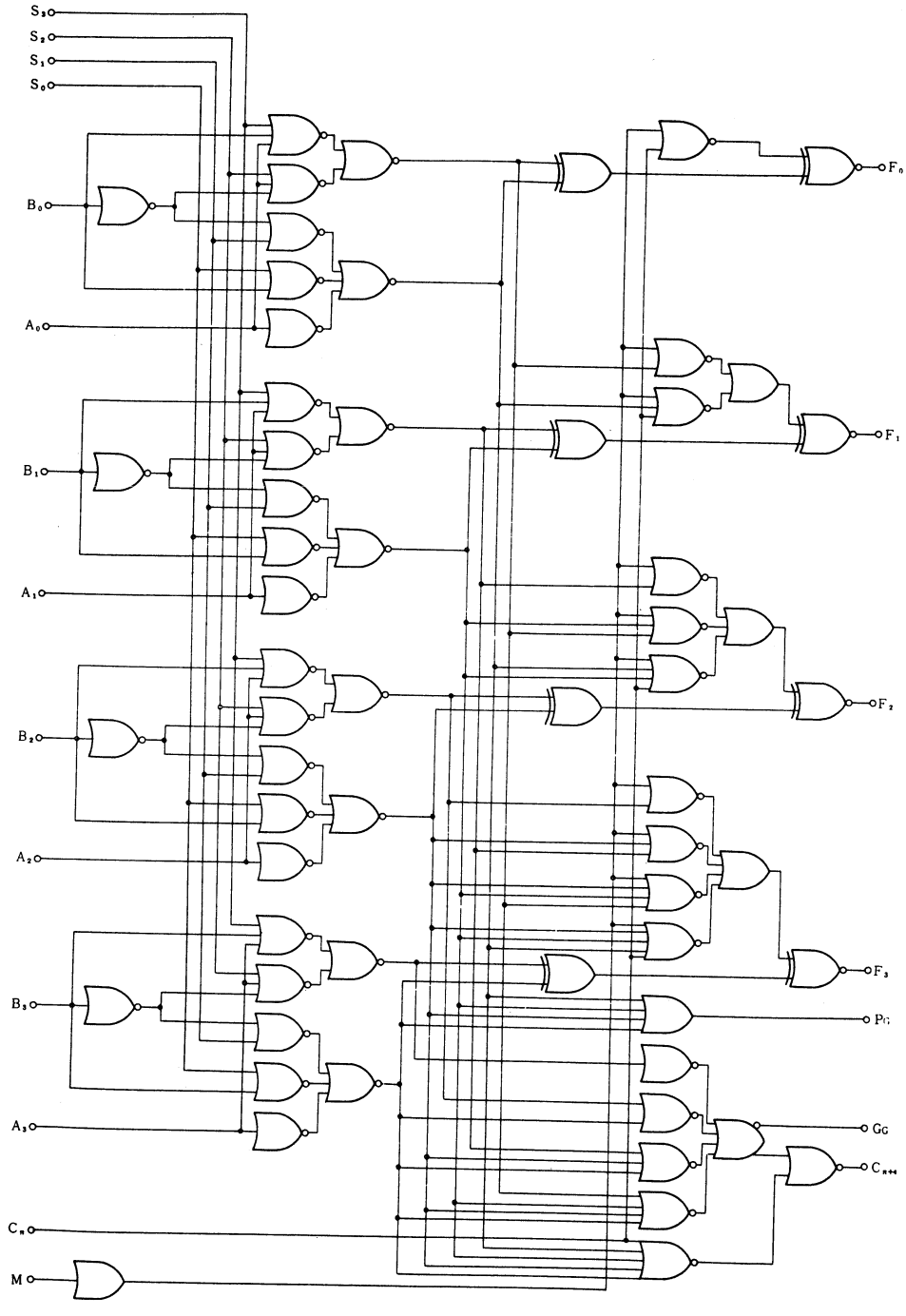
1. Positive Logic

Function Select				Logic Function (M="H")	Arithmetic Operation (M="L", Cn="L")
$\overline{S}_3$	$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	F	F
L	L	L	L	$F=\overline{A}$	$F=A+0$
L	L	L	H	$F=\overline{A}+\overline{B}$	$F=A+(A\cdot\overline{B})$
L	L	H	L	$F=\overline{A}+B$	$F=A+(A\cdot B)$
L	L	H	H	F="H"	$F=A\times 2$
L	H	L	L	$F=\overline{A\cdot B}$	$F=(A+B)+0$
L	H	L	H	$F=\overline{B}$	$F=(A+B)+(A\cdot\overline{B})$
L	H	H	L	$F=A\cdot B$	$F=A+B$
L	H	H	H	$F=A+\overline{B}$	$F=A+(A+B)$
H	L	L	L	$F=\overline{A}\cdot B$	$F=(A+\overline{B})+0$
H	L	L	H	$F=A\oplus B$	$F=A-B-1$
H	L	H	L	$F=B$	$F=(A+\overline{B})+(A\cdot B)$
H	L	H	H	$F=A+B$	$F=(A+\overline{B})+A$
H	H	L	L	F="L"	$F=-1$ (two's complement)
H	H	L	H	$F=A\cdot\overline{B}$	$F=(A\cdot\overline{B})-1$
H	H	H	L	$F=A\cdot B$	$F=(A\cdot B)-1$
H	H	H	H	$F=A$	$F=A-1$

2. Negative Logic

Function Select				Logic Function (M="H")	Arithmetic Operation (M="L", Cn="H")
S_3	S_2	S_1	S_0	F	F
L	L	L	L	$F=\overline{A}$	$F=A-1$
L	L	L	H	$F=\overline{A+B}$	$F=A+(A+\overline{B})$
L	L	H	L	$F=\overline{A}\cdot B$	$F=A+(A+B)$
L	L	H	H	F="L"	$F=A\times 2$
L	H	L	L	$F=\overline{A\cdot B}$	$F=(A\cdot B)-1$
L	H	L	H	$F=\overline{B}$	$F=(A\cdot B)+(A+\overline{B})$
L	H	H	L	$F=A\oplus B$	$F=A+B$
L	H	H	H	$F=A\cdot\overline{B}$	$F=A+(A\cdot B)$
H	L	L	L	$F=\overline{A}+B$	$F=(A\cdot\overline{B})-0$
H	L	L	H	$F=A\cdot B$	$F=A-B-1$
H	L	H	L	$F=B$	$F=(A\cdot\overline{B})+(A+B)$
H	L	H	H	$F=A\cdot B$	$F=(A\cdot\overline{B})+A$
H	H	L	L	F="H"	$F=-1$ (two's complement)
H	H	L	H	$F=A+\overline{B}$	$F=(A+\overline{B})+0$
H	H	H	L	$F=A+B$	$F=(A+B)+0$
H	H	H	H	$F=A$	$F=A+0$

BLOCK DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	—	145	mA
Input Current	I_{IH}	V_{IH} = −0.810V	B_0, B_1, B_2, B_3	25°C	—	—	245	μA
			A_0, A_1, A_2, A_3		—	—	220	
			S_3, M		—	—	200	
			S_0, S_1, S_2		—	—	265	
			C_n		—	—	290	
	I_{IL}	V_{IL} = −1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V, V_{IL} = −1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V, V_{IL} = −1.850V		25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V, V_{IL} = −1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IH} = −0.890V, V_{IL} = −1.890V		−30°C	−2.000	—	−1.675	V
		V_{IH} = −0.810V, V_{IL} = −1.850V		25°C	−1.990	—	−1.650	
		V_{IH} = −0.700V, V_{IL} = −1.825V		85°C	−1.920	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V, V_{ILA} = −1.500V		−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V, V_{ILA} = −1.475V		25°C	−0.980	—	—	
		V_{IHA} = −1.035V, V_{ILA} = −1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{IHA} = −1.205V, V_{ILA} = −1.500V		−30°C	—	—	−1.655	V
		V_{IHA} = −1.105V, V_{ILA} = −1.475V		25°C	—	—	−1.630	
		V_{IHA} = −1.035V, V_{ILA} = −1.440V		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C, R_L = 50Ω)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	C_n	C_{n+4}	A_0, A_1, A_2, A_3	−30°C	1.0	—	5.1	ns
					25°C	1.1	3.1	5.0	
					85°C	1.1	—	5.4	
	t_{PHL}				−30°C	1.0	—	5.1	
					25°C	1.1	3.1	5.0	
					85°C	1.1	—	5.4	
Rise Time	t_{TLH}				−30°C	1.0	—	3.2	
					25°C	1.0	2.0	3.0	
					85°C	1.0	—	3.2	
Fall Time	t_{THL}				−30°C	1.0	—	3.2	
					25°C	1.0	2.0	3.0	
					85°C	1.0	—	3.2	
Propagation Delay Time	t_{PLH}	C_n	F_1	A_0	−30°C	1.7	—	7.2	
					25°C	2.0	4.5	7.0	
					85°C	2.0	—	7.5	
	t_{PHL}				−30°C	1.7	—	7.2	
					25°C	2.0	4.5	7.0	
					85°C	2.0	—	7.5	
Rise Time	t_{TLH}				−30°C	1.3	—	5.3	
					25°C	1.5	3.0	5.0	
					85°C	1.5	—	5.3	
Fall Time	t_{THL}				−30°C	1.3	—	5.3	
					25°C	1.5	3.0	5.0	
					85°C	1.5	—	5.3	

(to be continued)

■ AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85℃$, $R_L=50\,\Omega$)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	A_1	F_1	—	−30℃	2.6	—	10.4	ns
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
	t_{PHL}				−30℃	2.6	—	10.4	
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
Rise Time	t_{TLH}				−30℃	1.3	—	5.4	
					25℃	1.5	3.0	5.0	
					85℃	1.5	—	5.3	
Fall Time	t_{THL}				−30℃	1.3	—	5.4	
					25℃	1.5	3.0	5.0	
					85℃	1.5	—	5.3	
Propagation Delay Time	t_{PLH}	A_1	P_G	S_0, S_3	−30℃	1.6	—	7.0	
					25℃	2.0	5.0	6.5	
					85℃	2.0	—	7.0	
	t_{PHL}				−30℃	1.6	—	7.0	
					25℃	2.0	5.0	6.5	
					85℃	2.0	—	7.0	
Rise Time	t_{TLH}				−30℃	0.8	—	3.7	
					25℃	1.1	2.0	3.5	
					85℃	1.1	—	3.8	
Fall Time	t_{THL}				−30℃	0.8	—	3.7	
					25℃	1.1	2.0	3.5	
					85℃	1.1	—	3.8	
Propagation Delay Time	t_{PLH}	A_1	G_G	A_0, A_2, A_3, C_n	−30℃	1.1	—	7.4	
					25℃	2.0	4.5	7.0	
					85℃	1.3	—	7.7	
	t_{PHL}				−30℃	1.1	—	7.4	
					25℃	2.0	4.5	7.0	
					85℃	1.3	—	7.7	
Rise Time	t_{TLH}				−30℃	1.2	—	5.1	
					25℃	1.5	4.0	5.0	
					85℃	1.2	—	5.3	
Fall Time	t_{THL}				−30℃	1.2	—	5.1	
					25℃	1.5	4.0	5.0	
					85℃	1.2	—	5.3	
Propagation Delay Time	t_{PLH}	A_1	C_{n+4}	A_0, A_2, A_3, C_n	−30℃	1.7	—	7.3	
					25℃	2.0	5.0	7.0	
					85℃	2.0	—	7.8	
	t_{PHL}				−30℃	1.7	—	7.3	
					25℃	2.0	5.0	7.0	
					85℃	2.0	—	7.8	
Rise Time	t_{TLH}				−30℃	1.0	—	3.1	
					25℃	1.0	2.0	3.0	
					85℃	1.0	—	3.2	
Fall Time	t_{THL}				−30℃	1.0	—	3.1	
					25℃	1.0	2.0	3.0	
					85℃	1.0	—	3.2	

(to be continued)

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85℃$, $R_L=50\,\Omega$)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	B_1	F_1	S_3, C_n	−30℃	2.7	—	11.3	ns
					25℃	3.0	8.0	11.0	
					85℃	3.0	—	11.9	
Rise Time	t_{TLH}				−30℃	1.2	—	5.3	
					25℃	1.5	3.5	5.0	
					85℃	1.5	—	5.3	
Fall Time	t_{THL}				−30℃	1.2	—	5.3	
					25℃	1.5	3.5	5.0	
					85℃	1.5	—	5.3	
Propagation Delay Time	t_{PLH}	B_1	P_G	S_0, S_3	−30℃	1.6	—	7.7	
					25℃	2.0	6.0	7.5	
					85℃	2.0	—	8.0	
	t_{PHL}				−30℃	1.6	—	7.7	
					25℃	2.0	6.0	7.5	
					85℃	2.0	—	8.0	
Rise Time	t_{TLH}				−30℃	1.0	—	3.6	
					25℃	1.1	2.0	3.5	
					85℃	1.1	—	3.9	
Fall Time	t_{THL}				−30℃	1.0	—	3.6	
					25℃	1.1	2.0	3.5	
					85℃	1.1	—	3.9	
Propagation Delay Time	t_{PLH}	B_1	G_G	S_3, C_n	−30℃	1.7	—	8.2	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.6	
	t_{PHL}				−30℃	1.7	—	8.2	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.6	
Rise Time	t_{TLH}				−30℃	1.4	—	5.2	
					25℃	1.5	3.0	5.0	
					85℃	1.2	—	5.4	
Fall Time	t_{THL}				−30℃	1.4	—	5.2	
					25℃	1.5	3.0	5.0	
					85℃	1.2	—	5.4	
Propagation Delay Time	t_{PLH}	B_1	C_{n+4}	S_3, C_n	−30℃	1.8	—	8.2	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.7	
	t_{PHL}				−30℃	1.8	—	8.2	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.7	
Rise Time	t_{TLH}				−30℃	0.9	—	3.1	
					25℃	1.0	2.0	3.0	
					85℃	1.0	—	3.2	
Fall Time	t_{THL}				−30℃	0.9	—	3.1	
					25℃	1.0	2.0	3.0	
					85℃	1.0	—	3.2	

(to be continued)

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85℃$, $R_L=50\Omega$)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	M	F_1	—	−30℃	2.4	—	10.3	ns
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
	t_{PHL}				−30℃	2.4	—	10.3	
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
Rise Time	t_{TLH}				−30℃	1.1	—	5.1	
					25℃	1.5	4.0	5.0	
					85℃	1.5	—	5.3	
Fall Time	t_{THL}				−30℃	1.1	—	5.1	
					25℃	1.5	4.0	5.0	
					85℃	1.5	—	5.3	
Propagation Delay Time	t_{PLH}	S_1	F_1	A_1, B_1	−30℃	2.5	—	10.7	
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
	t_{PHL}				−30℃	2.5	—	10.7	
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
Rise Time	t_{TLH}				−30℃	1.0	—	5.4	
					25℃	1.5	3.0	5.0	
					85℃	1.5	—	5.4	
Fall Time	t_{THL}				−30℃	1.0	—	5.4	
					25℃	1.5	3.0	5.0	
					85℃	1.5	—	5.4	
Propagation Delay Time	t_{PLH}	S_1	P_G	A_3, B_3	−30℃	1.7	—	8.3	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.4	
	t_{PHL}				−30℃	1.7	—	8.3	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.4	
Rise Time	t_{TLH}				−30℃	0.8	—	5.1	
					25℃	1.1	3.0	5.0	
					85℃	1.1	—	5.2	
Fall Time	t_{THL}				−30℃	0.8	—	5.1	
					25℃	1.1	3.0	5.0	
					85℃	1.1	—	5.2	
Propagation Delay Time	t_{PLH}	S_1	C_{n+4}	A_3, B_3	−30℃	1.6	—	9.3	
					25℃	2.0	6.0	9.0	
					85℃	2.0	—	9.9	
	t_{PHL}				−30℃	1.6	—	9.3	
					25℃	2.0	6.0	9.0	
					85℃	2.0	—	9.9	
Rise Time	t_{TLH}				−30℃	0.9	—	5.3	
					25℃	1.1	3.0	5.0	
					85℃	1.0	—	5.2	
Fall Time	t_{THL}				−30℃	0.9	—	5.3	
					25℃	1.1	3.0	5.0	
					85℃	1.0	—	5.2	

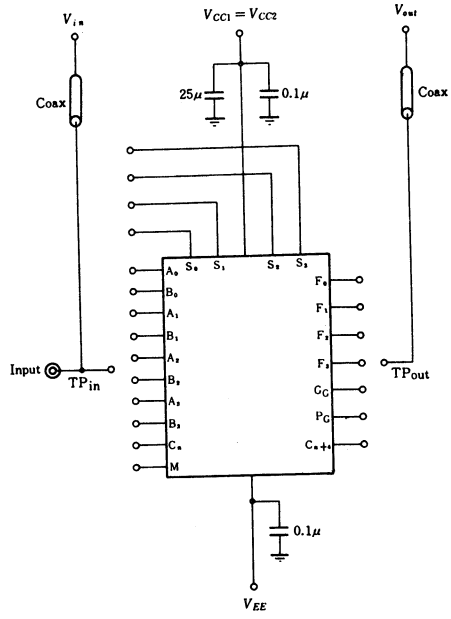
(to be continued)

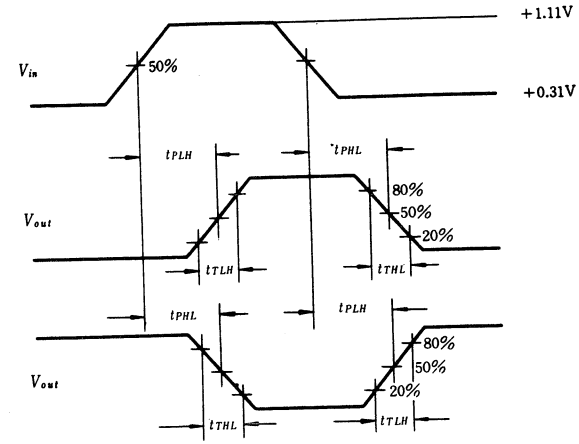
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$, $R_L=50\Omega$)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	S_1	G_G	A_3, B_3	−30°C	1.5	—	9.6	ns
					25°C	2.0	6.0	9.0	
					85°C	1.9	—	9.7	
	t_{PHL}				−30°C	1.5	—	9.6	
					25°C	2.0	6.0	9.0	
					85°C	1.9	—	9.7	
Rise Time	t_{TLH}				−30°C	0.8	—	6.2	
					25°C	0.8	3.0	6.0	
					85°C	0.8	—	6.5	
Fall Time	t_{THL}				−30°C	0.8	—	6.2	
					25°C	0.8	3.0	6.0	
					85°C	0.8	—	6.5	

Note) * : Other inputs are open, or connected to +0.31V.

■SWITCHING TIME TEST CIRCUIT



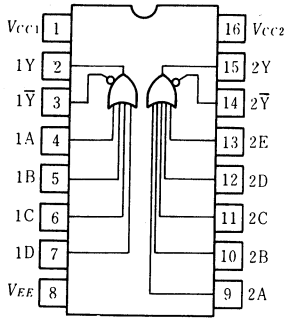


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

HD10209

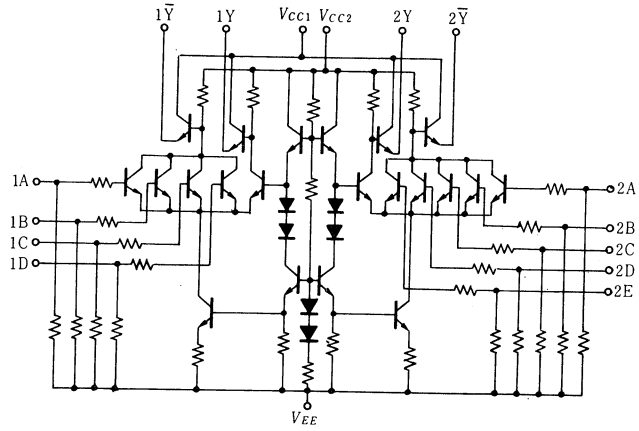
Dual 4-5-input OR/NOR Gates

■ PIN ARRANGEMENT



(Top View)

■ CIRCUIT SCHEMATIC



■ DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	11	14	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850V$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

■ AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=25°C$)

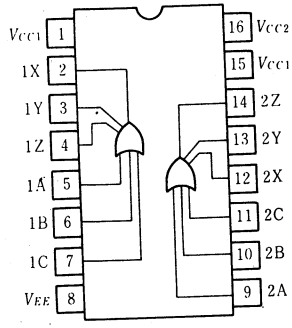
Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	0.95	—	1.55	ns
	t_{PHL}		0.95	—	1.55	
Rise/Fall Time	t_{TLH}		0.90	—	2.50	
	t_{THL}		0.90	—	2.50	

Note) Please refer to test circuit and waveform of common item.

HD10210

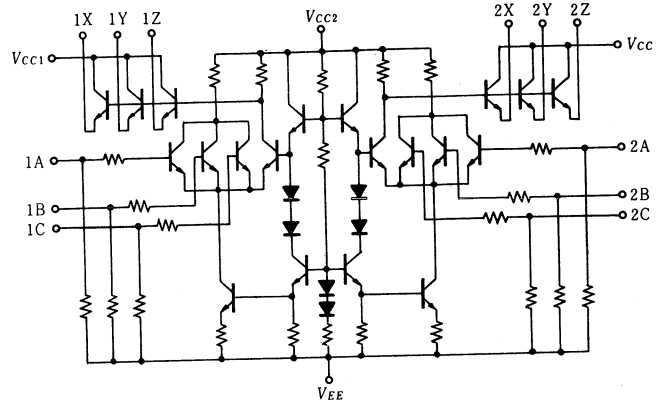
Dual 3-input 3-output OR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	30	38	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	410	μA
	I_{IL}	$V_{IL}=-1.850V$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

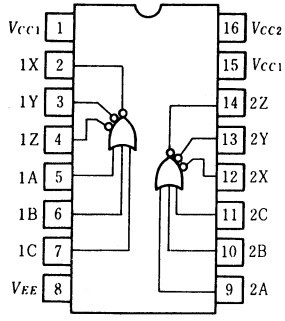
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=25°C$)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	0.95	1.5	2.5	ns
	t_{PHL}		0.95	1.5	2.5	
Rise/Fall Time	t_{TLH}		0.90	1.5	2.5	
	t_{THL}		0.90	1.5	2.5	

Note) Please refer to test circuit and waveform of common item.

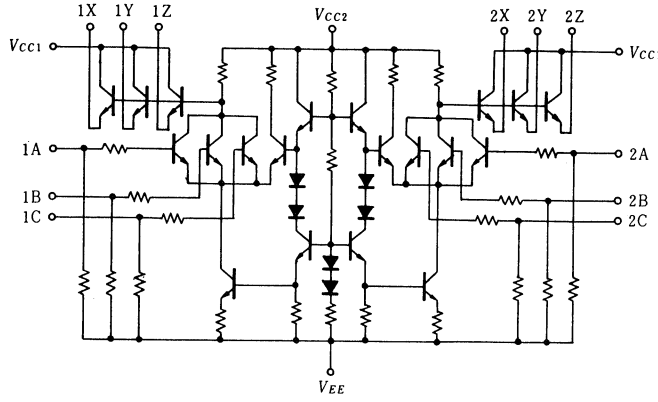
Dual 3-input 3-output NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	—	38	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	410	μA
	I_{IL}	$V_{IL}=-1.850V$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−0.960	—	−0.810	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−1.850	—	−1.650	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	−1.080	—	—	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	−0.980	—	—	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	—	—	−1.655	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	—	—	−1.630	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=25°C$)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50Ω$	0.95	1.5	2.5	ns
	t_{PHL}		0.95	1.5	2.5	
Rise/Fall Time	t_{TLH}		0.90	1.5	2.5	
	t_{THL}		0.90	1.5	2.5	

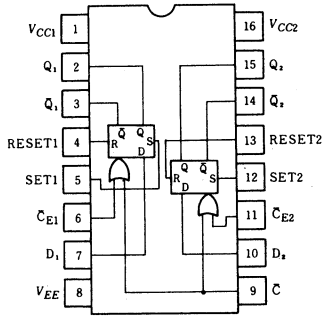
Note) Please refer to test circuit and waveform of common item.

HD10230

High Speed Dual D-type Latches

The HD10230 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock($\overline{C}$). Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

■PIN ARRANGEMENT



(Top View)

■FUNCTION

D	$\overline{C}$	$\overline{C}_E$	Q_{n+1}
L	L	L	L
H	L	L	H
×	L	H	Q_n
×	H	L	Q_n
×	H	H	Q_n

× : Don't Care

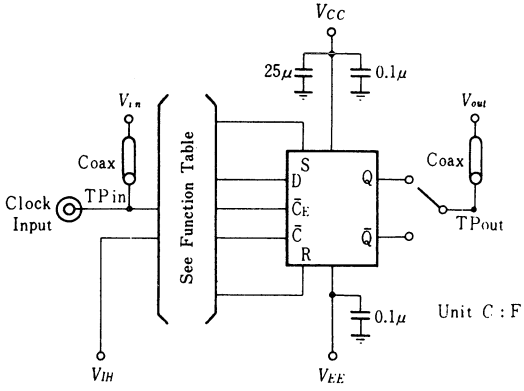
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

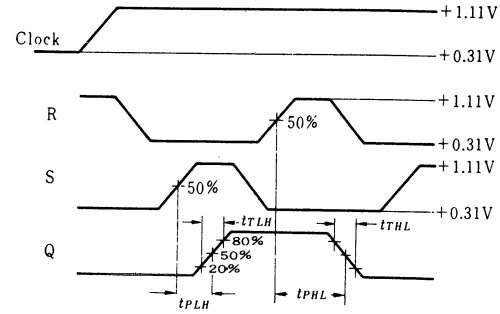
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	—	41	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	$\overline{C}_E$	25°C	—	—	255	μA
			$\overline{C}$		—	—	310	
			Other inputs		—	—	355	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

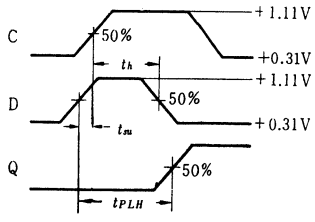
■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$\overline{C}$, $\overline{C}_E$	Q, $\overline{Q}$	R_L=50Ω, C_L=3.5pF	—	1.2	2.0	ns
	t_{PHL}				—	1.2	2.0	
	t_{PLH}	D	Q, $\overline{Q}$		—	1.0	1.8	
	t_{PHL}				—	1.0	1.8	
	t_{PLH}	S, R	Q, $\overline{Q}$		—	1.2	2.0	
	t_{PHL}				—	1.2	2.0	
Rise/Fall Time	t_{TLH}	—	Q, $\overline{Q}$		—	1,5	2.5	ns
	t_{THL}				—	1.5	2.5	
Setup Time	t_{su}	$\overline{C}$→D	Q, $\overline{Q}$		—	—	2.0	ns
Hold Time	t_h				—	—	1.0	ns

■ SWITCHING TIME TEST CIRCUIT







Notes)

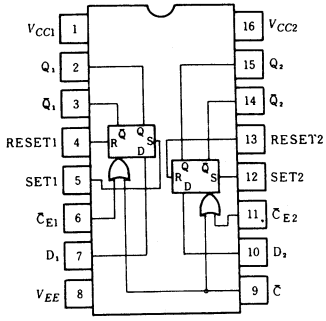
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope and equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.
5. Input Pulse; t_{TLH}=t_{THL}=1.5±0.2ns (20% to 80%).

HD10231

High Speed Dual D-type Master-Slave Flip Flops

The HD10231 is a dual master-slave type D flip-flop. Asynchronous Set(S) and Reset(R) override Clock ($\overline{C_C}$) and Clock Enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock. The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data(D) input will not affect the output information at any other time due to master-slave construction.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

● R-S

R	S	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	Q_n	$\overline{Q}_n$
L	H	H	L
H	L	L	H
H	H	×	×

× : Don't Care

● CLOCK

C	D	Q_{n+1}
L	×	Q_n
↑	L	L
↑	H	H

1. × : Don't Care
2. $C = \overline{C}_E + \overline{C}_C$
3. ↑ : transition from low to high

■DC CHARACTERISTICS ($V_{EE} = -5.2V$, $Ta = -30 \sim +85°C$)

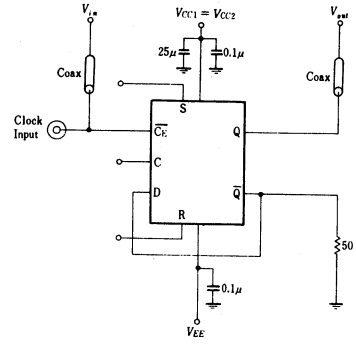
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	52	65	mA
Input Current	I_{IH}	$V_{IH} = -0.810V$	D, $\overline{C_E}$	25°C	—	—	220	μA
			$\overline{C}$		—	—	290	
			S, R		—	—	410	
	I_{IL}	$V_{IL} = -1.850V$		25°C	—	—	0.5	μA
Output Voltage	V_{OH}	$V_{IH} = -0.890V$ or $V_{IL} = -1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH} = -0.810V$ or $V_{IL} = -1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH} = -0.700V$ or $V_{IL} = -1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL} = -1.890V$ or $V_{IH} = -0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL} = -1.850V$ or $V_{IH} = -0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL} = -1.825V$ or $V_{IH} = -0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA} = -1.205V$ or $V_{ILA} = -1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA} = -1.105V$ or $V_{ILA} = -1.475V$		25°C	−0.980	—	—	
		$V_{IHA} = -1.035V$ or $V_{ILA} = -1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA} = -1.500V$ or $V_{IHA} = -1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA} = -1.475V$ or $V_{IHA} = -1.105V$		25°C	—	—	−1.630	
		$V_{ILA} = -1.440V$ or $V_{IHA} = -1.035V$		85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$\overline{C}$, $\overline{C}_E$	Q, $\overline{Q}$	R_L=50Ω,	−30°C	1.4	—	3.4	ns
					25°C	1.5	—	3.3	
					85°C	1.5	—	3.7	
	t_{PHL}				−30°C	1.4	—	3.4	
					25°C	1.5	—	3.3	
					85°C	1.5	—	3.7	
	t_{PLH}	S	Q, $\overline{Q}$		−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
	t_{PHL}				−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
	t_{PLH}	R	Q, $\overline{Q}$		−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
	t_{PHL}				−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
Rise Time	t_{TLH}		Q, $\overline{Q}$		−30°C	0.9	—	3.3	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.5	
Fall Time	t_{THL}				−30°C	0.9	—	3.3	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.5	
Setup Time	t_{su}	D → $\overline{C}$	Q, $\overline{Q}$		25°C	—	—	1.0	ns
Hold Time	t_h				25°C	—	—	0.75	ns
Max. Toggle Frequency	f_{Tog}	—	—		−30°C	200	—	—	MHz
					25°C	200	250	—	
					85°C	200	—	—	

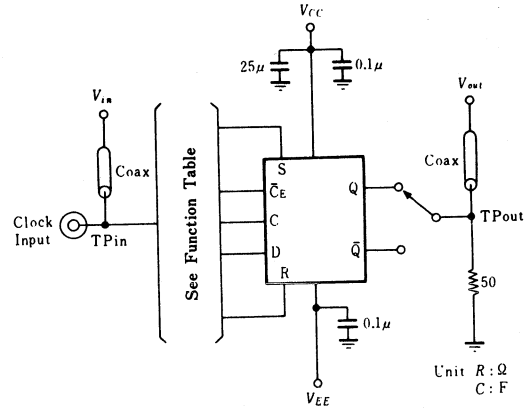
■ TEST CIRCUIT OF AC CHARACTERISTICS

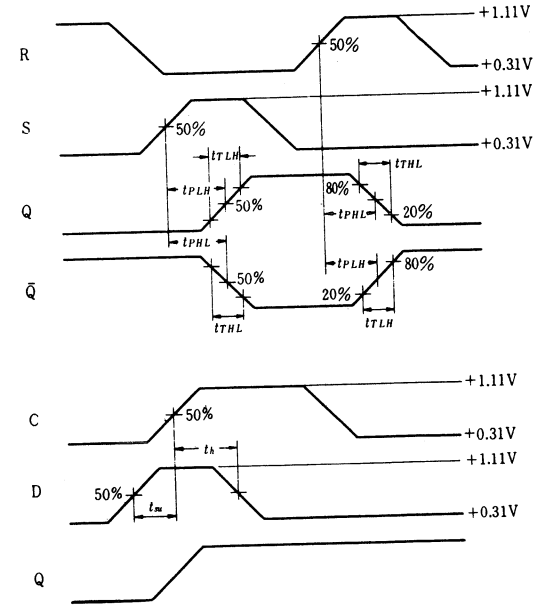
1. Toggle Frequency



Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin TPout to output pin.

2. Switching Time





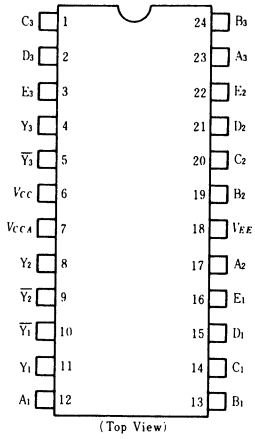
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at data.
5. Input Pulse; t_{TLH}=t_{THL}=1.5±0.2ns (20% to 80%).

HD100K Series

HD100101

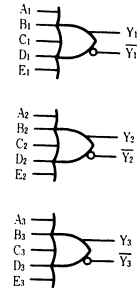
Triple 5-input OR/NOR Gates

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		18	26	38	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$		—	—	350	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}		$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$°C)

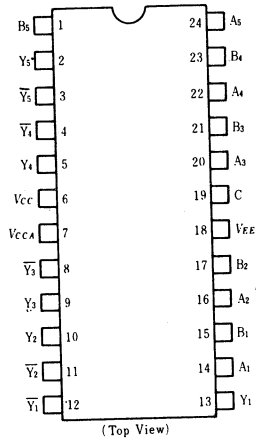
Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveforms	0.45	0.75	1.35	ns
	t_{PHL}					
Transition Time	t_{TLH}		0.35	0.70	1.30	ns
	t_{THL}					

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100102

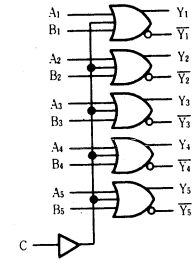
Quintuple 2-input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			38	55	80	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	pin 19		—	—	300	μA
			All input except pin 19		—	—	350	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		$R_L=50\Omega$ $V_{TT}=-2.0V$	−1025	−955	−880	mV
	V_{OL}				−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_L=50\Omega$ $V_{TT}=-2.0V$	−1035	—	—	mV
	V_{OLC}				—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5V$, $V_{CC}=2.0V$, $Ta=25°C$)

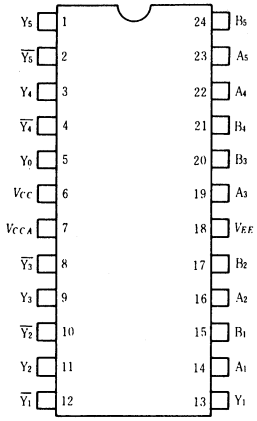
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveforms	All input except pin 19	0.45	0.75	1.35	ns
			pin 19	0.90	1.50	2.20	ns
Transition Time	t_{TLH} t_{THL}		pin 19	0.40	0.70	1.35	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100107

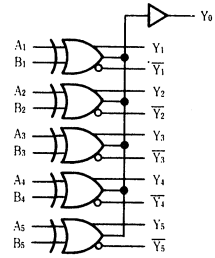
Quintuple Exclusive-OR/NOR Gates

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			46	66	96	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	Pin 24, 15, 17, 20, 21		—	—	250	μA
			Pin 22, 23, 14, 16, 19		—	—	350	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$		R_L = 50Ω	−1025	−955	−880	mV
	V_{OL}			V_{TT} = −2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$		R_L = 50Ω	−1035	—	—	mV
	V_{OLC}			V_{TT} = −2.0V	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

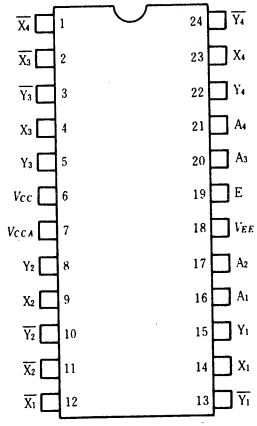
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveforms	Pin 24, 15, 17, 20, 21	0.55	1.10	1.85	ns
			Pin 22, 23, 14, 16, 19	0.55	0.90	1.70	ns
			Pin 5	1.10	1.85	2.65	ns
Transition Time	t_{TLH} t_{THL}			0.40	0.70	1.35	ns

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100112

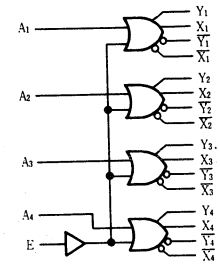
Quadruple Drivers

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			51	73	106	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	Pin 19		—	—	450	μA
			All input except pin 19		—	—	550	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}			$V_{TT}=-2.0V$	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}			$V_{TT}=-2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS ($V_{EE}=-2.5V$, $V_{CC}=2.0V$, $Ta=25°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	Enable(Common input)	0.85	1.30	1.85	ns
	t_{PHL}		Data	0.55	0.90	1.55	ns
Transition Time	t_{TLH}			0.45	0.90	1.80	ns
	t_{THL}						

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

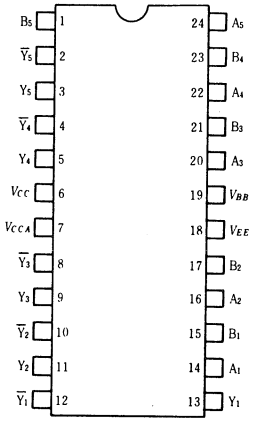
HD100114

Quint. Differential Line Receivers

The HD100114 is a Quint. Differential Amp. with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single ended reception. Active current sources provide common mode rejection of 1.5V in either the positive or negative direction.

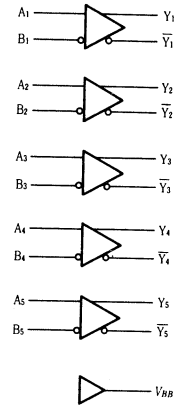
A defined output state exists if both inputs are at the same potential between and including $-V_{EE}$ and V_{CC}. The defined state is logic high on outputs $\overline{Y}n$.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Input		Output	
A_n	B_n	Y_n	$\overline{Y_n}$
H	V_{BB}	H	L
L	V_{BB}	L	H
V_{BB}	H	L	H
V_{BB}	L	H	L
$A_n - B_n \geq 0.15$ V		H	L
$A_n - B_n \leq 0.0$ V		L	H
$0.0 < A_n - B_n < 0.15$ V		*	*
Open	Open	L	H
V_{CC}	V_{CC}	L	H
V_{EE}	V_{EE}	L	H

H = High level
L = Low level
V_{BB} = Base bias voltage
* = Undefined

■ DC CHARACTERISTICS ($V_{EE} = -4.5$V, $V_{CC} =$ GND, $Ta = 0 \sim +85$°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	$A_n = V_{BB}$, $B_n = V_{IL\ min}$	51	73	106	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$, $A_n = V_{BB}$, $B_n = V_{IL\ min}$	—	20	50	μA
Leakage Current	I_{CBO}	$V_{IN} = V_{EE}$, $A_n = V_{BB}$, $B_n = V_{IL\ min}$	—	—	1.0	μA
Common Mode Voltage	V_{CM}	Permissible V_{CM} with respect to V_{BB}	−2.30	—	−0.55	V
Reference Voltage	V_{BB}	Tie pins 22, 24, 14, 16, 20 to pin 19	−1380	−1320	−1260	mV
Input Voltage Differential	V_{DIFF}		—	150	—	mV

■ AC CHARACTERISTICS ($V_{EE} = -2.5$V, $V_{CC} = 2.0$V, $Ta = 25$°C)

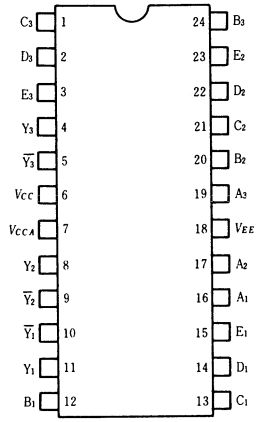
Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	0.65	1.20	2.10	ns
Transition Time	t_{THL} t_{TLH}		0.30	0.90	1.40	ns

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100117

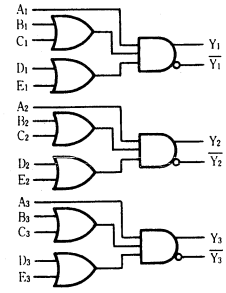
Triple 2-wide OR-AND/OR-AND-INVERT Gates

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		37	54	79	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	Pin 16, 17, 19	—	—	350	μA
			All input except pin 16, 17, 19	—	—	220	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$	R_L = 50Ω	−1025	−955	−880	mV
	V_{OL}		V_{TT} = −2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$	R_L = 50Ω	−1035	—	—	mV
	V_{OLC}		V_{TT} = −2.0V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

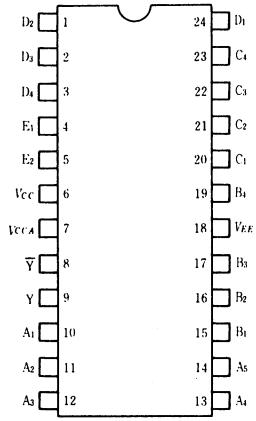
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	All input except pin 16, 17, 19	0.90	1.70	2.40	ns
	t_{PHL}		Pin 16, 17, 19	0.45	0.75	1.30	ns
Transition Time	t_{TLH}			0.30	0.75	1.30	ns
	t_{THL}						

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100118

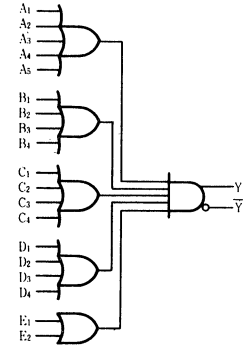
5-wide OR-AND/OR-AND-INVERT Gates

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			27	39	57	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	A input		—	—	350	μA
			B~E input		—	—	240	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$		R_T = 50Ω	−1025	−955	−880	mV
	V_{OL}			V_{TT} = −2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$		R_T = 50Ω	−1035	—	—	mV
	V_{OLC}			V_{TT} = −2.0V	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

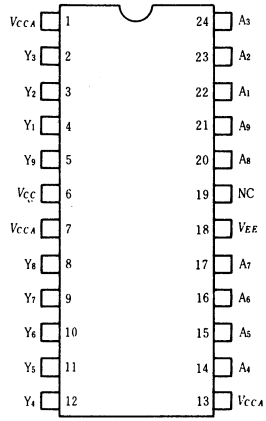
Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	0.95	1.40	1.90	ns
Transition Time	t_{TLH} t_{THL}		0.30	0.75	1.35	ns

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

9-bit Buffers

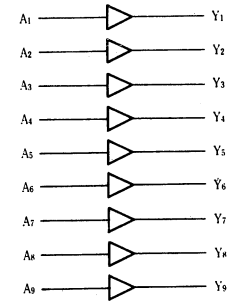
The HD100122 contains nine independent, high speed, buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus oriented systems where minimal output loading or bus isolation is desired.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



Note) NC ; No connection

■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		47	70	95.5	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$		—	—	350	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$	R_T = 50Ω	−1025	−955	−880	mV
	V_{OL}		V_{TT} = −2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$	R_T = 50Ω	−1035	—	—	mV
	V_{OLC}		V_{TT} = −2.0V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	0.45	0.90	1.55	ns
	t_{PHL}					
Transition Time	t_{TLH}		0.45	0.90	1.55	ns
	t_{THL}					

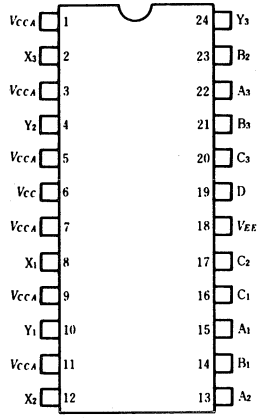
Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100123

Hex Bus Drivers

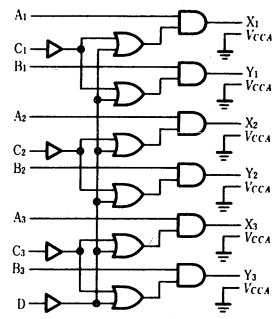
The HD100123 contains six bus drivers capable of driving terminated lines with terminations as low as 25Ω. To reduce crosstalk, each output has its respective ground connection and transition times were designed to be longer than on other HD100K devices.
The driver itself performs the positive logic AND of a data input (A, B inputs) and the OR of two select inputs (C, D inputs).
The output voltage low level is designed to be more negative than normal ECL outputs.
This allows an emitter-follower output transistor to turn off when the termination supply is −2.0V ±10%, and thus present a high impedance to the data bus.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			113	162	235	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	A, B, C input		—	—	230	μA
			D input		—	—	330	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or	R_T = 25Ω	V_{TT} = −2.0V	−1025	−955	−880	mV
	V_{OL}	$V_{IN}=V_{IL\ min}$		V_{TT} = −2.3V	—	—	−2200	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or	R_T = 25Ω	V_{TT} = −2.0V	−1035	—	—	mV
	V_{OLC}	$V_{IN}=V_{IL\ max}$		V_{TT} = −2.3V	—	—	−2200	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

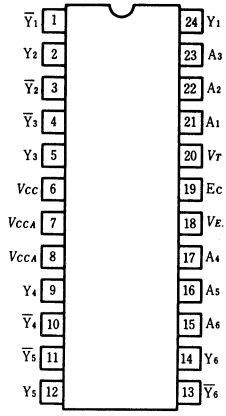
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	A, B input	1.85	3.00	4.20	ns
	t_{PHL}			1.00	1.45	2.20	
	t_{PLH}		C input	2.10	3.40	4.50	
	t_{PHL}			1.20	1.80	2.50	
	t_{PLH}		D input	2.20	3.50	4.90	
	t_{PHL}			1.20	1.80	2.65	
Transition Time	t_{TLH}			0.75	1.30	2.10	ns
	t_{THL}			0.40	0.80	1.20	

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Hex TTL-to-ECL Translators

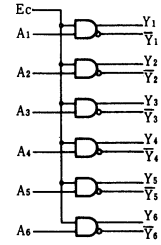
The HD100124 is a Hex Translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or with Schottky TTL. A Common Enable input (E_C), when low, holds all inverting outputs high and holds all True outputs low.
The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated. When the circuit is used in the differential mode, the HD100124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND, V_{TTL}=5.0V, Ta=0~+85°C)

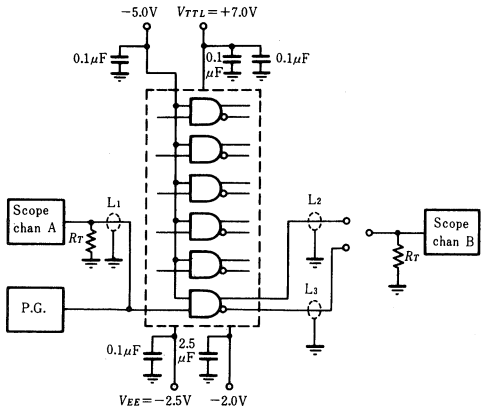
Item		Symbol	Test Condition	min	typ	max	Unit
Input Voltage		V_{IH}	Guaranteed Input Voltage High for All Inputs	2.0	—	5.0	V
		V_{IL}	Guaranteed Input Voltage Low for All Inputs	0	—	0.8	V
Clamp Input Voltage		V_{CD}	I_{IN}=−10mA	−1.5	—	—	V
Input Breakdown Voltage		V_{BO}	I_{IN}=1.0mA, Other Inputs V_{IN}=GND	5.5	—	—	V
Input Current	A inputs	I_{IH}	V_{IN}=2.4V, Ec V_{IN}=0.4V	—	—	50	μA
		I_{IL}	V_{IN}=0.4V, Ec V_{IN}=4.0V	−3.2	—	—	mA
	Ec input	I_{IHX}	Ec V_{IN}=2.4V, All Other Inputs V_{IN}=0.4V	—	—	300	μA
		I_{ILX}	Ec V_{IN}=0.4V, All Other Inputs V_{IN}=4.0V	−16.0	—	—	mA
Power Supply Current		I_{EE}	Inputs and Outputs Open	52	85	106	mA
		I_{CCH}	All Inputs V_{IN}=4.0V	—	41	56	mA
		I_{CCL}	All Inputs V_{IN}=GND	—	44	61	mA

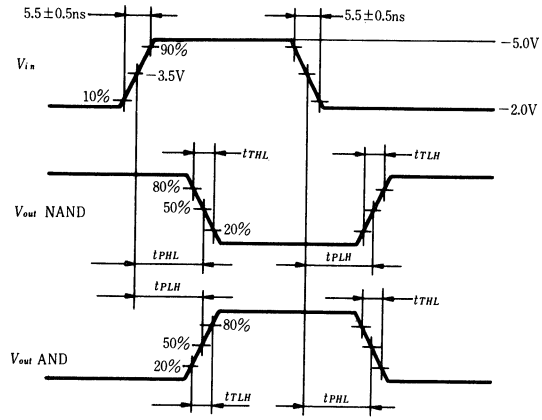
■ AC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND, V_{TTL}=5.0V, Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See Test Circuit and Waveform	0.50	1.60	3.00	ns
Transition Time	t_{TLH}, t_{THL}		0.60	1.20	2.50	ns

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

SWITHCING TIME TEST CIRCUIT AND WAVEFORM



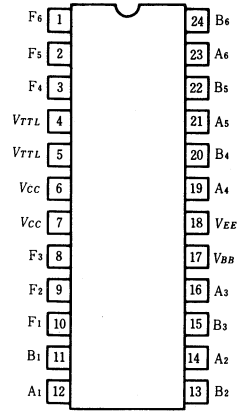


Notes) 1. L_1, L_2 and L_3 are equal lengths of 50Ω impedance lines
2. R_T equals 50Ω termination of scope

Hex ECL-to-TTL Translators

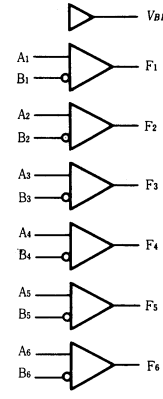
The HD100125 is a Hex Translator for converting HD100K logic levels to TTL logic levels. Differential inputs allow each circuits to be used as an inverting, non-inverting or as a differential receiver. An internal reference voltage generator provides V_{BB} on pin 17 for single-ended operation or for use in Schmitt trigger applications. The outputs, which will go low when the inputs are left unconnected, have a fan-out of 10 Schottky TTL loads. When used in the differential mode, the inputs have a common mode rejection of −1V, making this device tolerant of ground offsets and transients between the signal source and the translator.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Inputs		Output
In	$\overline{In}$	On
L	H	L
H	L	H
L	L	*
H	H	*
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

* Undetermind

■ DC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND=0V, V_{TTL}=5.0V, Ta=0∼+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	I_{OH}=−2.0mA	2.5	—	—	V
	V_{OL}		I_{OL}=20mA	—	—	0.5	V
	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	I_{OH}=−2.0mA	2.5	—	—	V
	V_{OLC}		I_{OL}=20mA	—	—	0.5	V
Common Mode Voltage	V_{CM}	V_{CM} ref. to V_{BB} (Notes 1)		—	—	1.0	V
Input Voltage Differential	V_{DIFF}	Required for full output voltage swing		150	—	—	mV
Reference Voltage	V_{BB}	$V_{IN}=V_{ILB}$		−1380	−1320	−1260	mV
Input Current	I_{IL}	$V_{IN}=V_{EE}$ (Notes 2)		−0.5	—	—	μA
	I_{IH}	$V_{IN}=V_{IHA}$ (Notes 2)		—	—	350	μA
Short Circuit Current	I_{OS}	V_{IN}=GND (Notes 3)		−100	—	−40	mA
Power Supply Current	I_{EE}	Inputs and Outputs Open		36	65	85	mA
TTL Drive Current	I_{TTL}	$V_{IN}=V_{ILB}$ (Notes 4)		50	88	115	mA

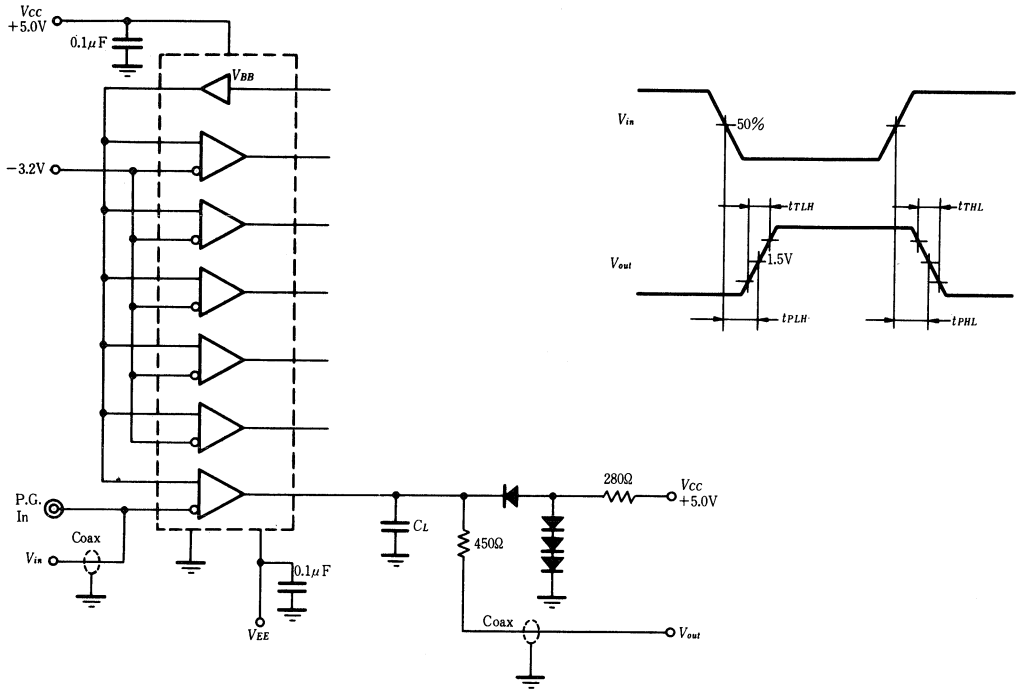
Notes) 1. $V_{CM}=V_{BB}\pm1V$ (V_{DIFF}=150mV)
2. Complementary Input = V_{BB}
3. One Output at a Time
4. True Inputs = V_{BB}, Complementary Inputs = V_{ILB}

AC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=0V, V_{TTL}=5.0V, Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See Test Circuit and Waveform	1.10	2.20	3.80	ns
Transition Time	t_{TLH}, t_{THL}		—	0.60	1.80	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

SWITHCING TIME TEST CIRCUIT AND WAVEFORM



Notes)
1. 50Ω termination to ground located in each scope channel input.
2. All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be <½ inch from TPin to input pin and TPout to output pin.
3. C_L=25pF including.
4. One input from each gate must be tied to V_{BB}.

HD100130

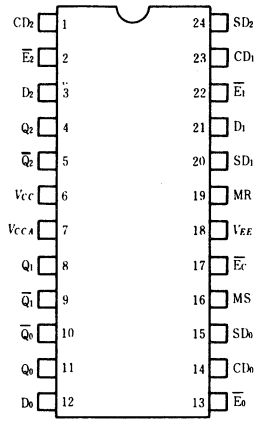
Triple D-type Latches

The HD100130 contains three D-type latches with true and complement outputs and with Common Enable ($\overline{Ec}$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{En}$), Direct Set (SDn) and Direct Clear (CDn) inputs.

The Q output follows its Data (D) input when both $\overline{En}$ and $\overline{Ec}$ are low. When either $\overline{En}$ or $\overline{Ec}$ or both are high, a latch stores the last valid data present on its Dn input before $\overline{En}$ or $\overline{Ec}$ when high. Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs.

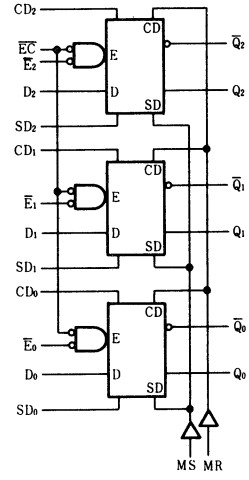
The individual CDn and SDn also override the Enable inputs.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

D_n	$\overline{E_n}$	$\overline{Ec}$	MS SD_n	MR CD_n	Q_n
L	L	L	L	L	L
H	L	L	L	L	H
×	H	×	L	L	*
×	×	H	L	L	*
×	×	×	H	L	H
×	×	×	L	H	L
×	×	×	H	H	U

H = High level
L = Low level
× = Immaterial
* = Ratains data present before $\overline{E}$ positive transition
U = Undefined

■ DC CHARACTERISTICS ($V_{EE}=-4.5$V, V_{CC}=GND, $Ta=0\sim+85$℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		61	88	128	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	D_n input	—	—	350	μA
			CD_n, SD_n input	—	—	530	
			$\overline{E_n}$ input	—	—	240	
			$\overline{Ec}$, MR, MS input	—	—	450	
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_T=50\Omega$ $V_{TT}=-2.0$V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_T=50\Omega$ $V_{TT}=-2.0$V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	Fig. 1	D_n input	0.50	0.85	1.35	ns
			CD_n, SD_n, $\overline{E_n}$ input	0.65	1.10	1.50	
			$\overline{Ec}$ input	0.70	1.20	1.65	
			MS, MR input	1.10	1.85	2.40	
Transition Time	t_{TLH}, t_{THL}			0.30	0.90	1.50	ns
Set-up Time	t_{su}	Fig. 2	D_n input	0.80	—	—	ns
			CD_n, SD_n input(Release Time)	1.40	—	—	
			MR, MS input(Release Time),	2.20	—	—	
Hold Time	t_h		D_n input	0	—	—	ns
Pulse Width	t_{pw}		$\overline{E_n}$, $\overline{Ec}$(Low)	1.20	—	—	ns
			CD_n, SD_n, MR, MS	1.35	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

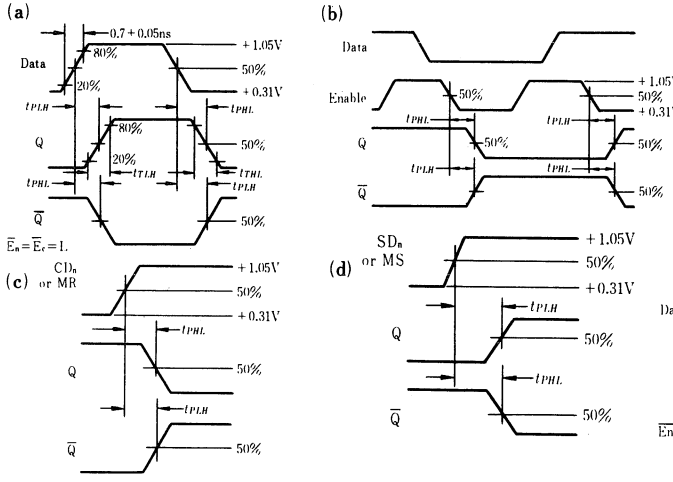


Fig.1 Propagation Delay Time

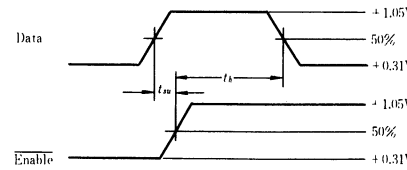
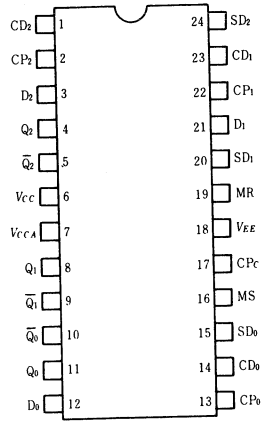


Fig.2 Set-up, and Hold Time

Triple D-type Flip-Flops

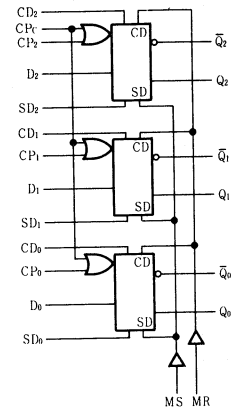
The HD100131 contains three D-type Master Slave Flip Flops with true and complement outputs, a Common Clock (CPc), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual clocks (CPn), Direct Set (SDn) and Direct Clear (CDn) inputs. Data enters a master when both CPn and CPc are low and transfers to a slave when CPn or CPc (or both) go high.
The Master Set, Master Reset and individual CDn and SDn inputs override the Clock inputs.

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■TRUTH TABLE

D_n	CP_n	CP_C	MS / SD_n	MR / CD_n	Q_{n+1}
L	↑	L	L	L	L
H	↑	L	L	L	H
L	L	↑	L	L	L
H	L	↑	L	L	H
×	H	×	L	L	Q_n
×	×	H	L	L	Q_n
×	×	×	H	L	H
×	×	×	L	H	L
×	×	×	H	H	U

H = High level
L = Low level
× = Immaterial
U = Undefined
↑ = Clock transition from low level to high level

■DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		74	106	149	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	CP_n, D_n input	—	—	240	μA
			MS, MR, CP_C input	—	—	450	
			CD_n, SD_n input	—	—	530	
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_T=50\Omega$, $V_{TT}=-2.0$ V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_T=50\Omega$, $V_{TT}=-2.0$ V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	Fig. 1	CP_C input	0.75	1.25	1.90	ns
			CD_n, SD_n input (CP=H)	0.80	1.55	2.20	
			CD_n, SD_n input (CP=L)	0.70	1.15	1.70	
			CP_n input	0.70	1.15	1.70	
			MS, MR input (CP=H)	1.05	1.90	2.85	
			MS, MR input (CP=L)	0.95	1.70	2.55	
Transition Time	t_{TLH} t_{THL}			0.35	0.90	1.50	ns
Set-up Time	t_{su}	Fig. 2	D_n input	0.80	—	—	ns
			CD_n, SD_n input (Release Time)	1.40	—	—	
			MS, MR input (Release Time)	2.20	—	—	
Hold Time	t_h		D_n input	0.20	—	—	ns
Toggle Frequency	f_{tog}	Fig. 3		300	—	—	MHz
Pulse Width	t_{pw}		CP_n, CP_C	0.95	—	—	ns
			CD_n, SD_n, MS, MR	1.35	—	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

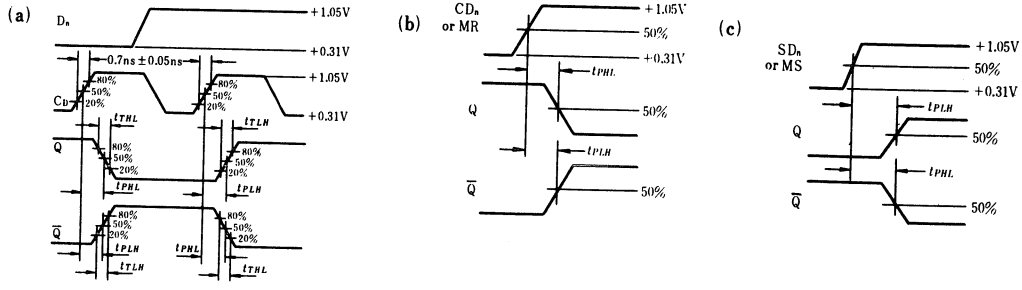


Fig.1 Propagation Delay Time

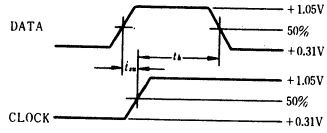


Fig.2 Set-up, and Hold Time

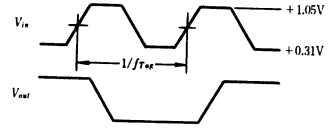


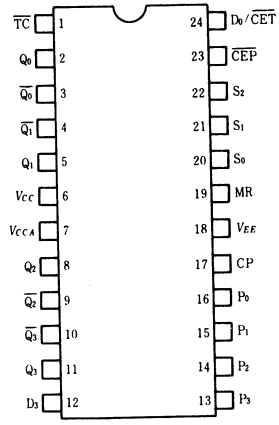
Fig.3 Toggle Frequency

4-stage Counters/Shift Registers

The HD100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (Sn) inputs determine the mode of operation, as shown in the mode select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multi-stage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (Do) input for shift-up operation.

For shift-down operation D_3 is the Serial Data input. In counting operation the Terminal Count ($\overline{TC}$) output goes low when the counter reaches 15 in the count/up mode or 0 in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the Do/$\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multi-stage counting or shift-up operation. The individual Preset (Pn) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A high signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, asynchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops.

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION SELECT TABLE

S_0	S_1	S_2	Function
L	L	L	Load
L	H	L	Shift down
H	H	L	Shift up
L	L	H	Count down
L	H	H	Count up
H	H	H	Hold
H	L	L	Complement
H	L	H	Clear

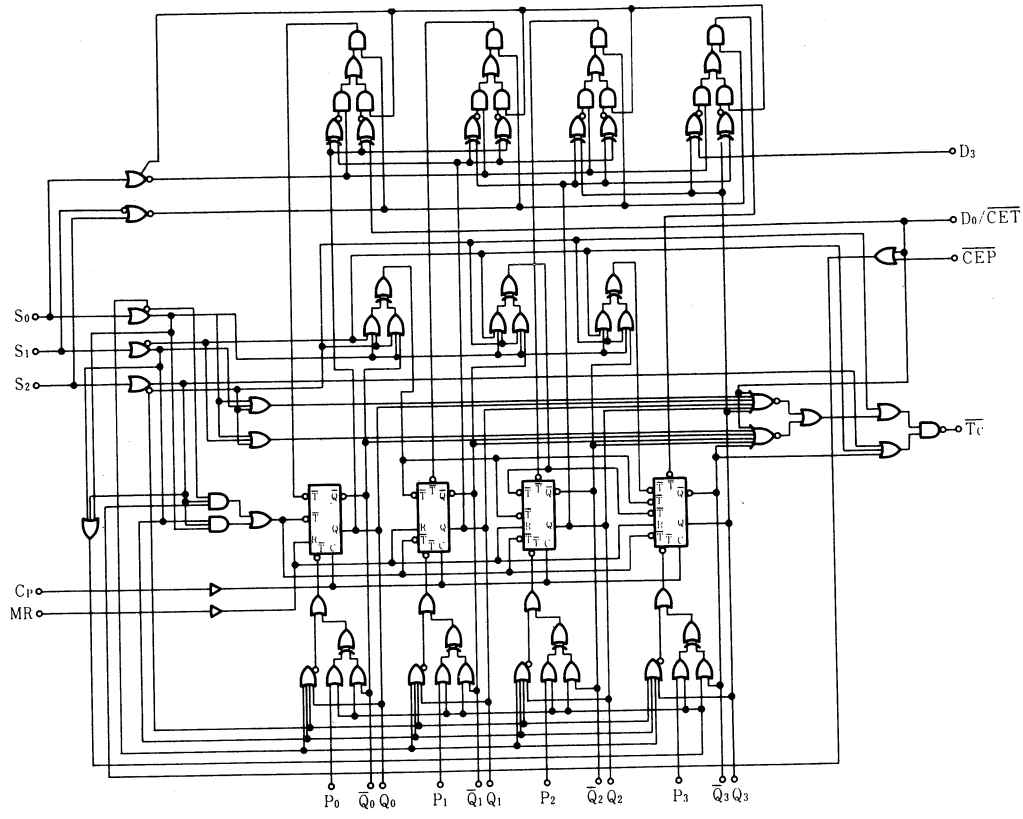
H = High level
L = Low level

TRUTH TABLE

IN												OUT					Mode
S_0	S_1	S_2	CP	MR	CEP	D_0/CET	D_3	P_3	P_2	P_1	P_0	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	
L	L	L	↑	L	×	×	×	H	L	H	H	H	L	H	H	L	Load *
H	H	H	↑	L	×	×	×	×	×	×	×	H	L	H	H	H	Hold
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	L	L	H	Count up (max)
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	L	H	H	
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	H	L	H	
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	H	H	L	
L	H	H	↑	L	L	L	×	×	×	×	×	L	L	L	L	H	
L	H	H	↑	L	L	L	×	×	×	×	×	L	L	L	H	H	
L	H	H	×	L	L	H	×	×	×	×	×	L	L	L	H	H	($\overline{CET}$ inhibit)
L	H	H	×	L	H	L	×	×	×	×	×	L	L	L	H	H	($\overline{CEP}$ inhibit)
×	×	×	×	H	×	×	×	×	×	×	×	L	L	L	L	×	Clear (MR)
L	L	L	↑	L	×	×	×	L	H	L	L	L	H	L	L	L	Load *
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	H	H	H	Count down (max)
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	H	L	H	
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	L	H	H	
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	L	L	L	
L	L	H	↑	L	L	L	×	×	×	×	×	H	H	H	H	H	
H	L	L	↑	L	×	×	×	×	×	×	×	H	H	H	L	H	
×	×	×	×	H	×	×	×	×	×	×	×	L	L	L	H	L	Complement
H	L	H	↑	L	×	×	×	×	×	×	×	L	L	L	L	×	Clear (MR)
H	H	L	↑	L	×	H	×	×	×	×	×	L	L	L	L	H	Clear
H	H	L	↑	L	×	L	×	×	×	×	×	L	L	L	H	L	Shift up
H	H	L	↑	L	×	H	×	×	×	×	×	L	L	H	L	L	
H	H	L	↑	L	×	L	×	×	×	×	×	L	H	L	H	L	
×	×	×	×	H	×	×	×	×	×	×	×	H	L	H	L	H	
L	H	L	↑	L	×	×	H	×	×	×	×	L	L	L	L	×	Clear (MR)
L	H	L	↑	L	×	×	L	×	×	×	×	H	L	L	L	H	Shift down
L	H	L	↑	L	×	×	H	×	×	×	×	L	H	L	L	L	
L	H	L	↑	L	×	×	L	×	×	×	×	H	L	H	L	H	
×	×	×	×	H	×	×	×	×	×	×	×	L	H	L	H	L	
												L	L	L	L	×	Clear (MR)

× = Immaterial
* = each LOAD data
↑ = CP positive transition

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		136	195	283	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	P_n, S_n input	—	—	180	μA
			$\overline{CEP}$ input	—	—	200	
			MR input	—	—	240	
			D_3 input	—	—	280	
			CP input	—	—	390	
			$D_0/\overline{CET}$ input	—	—	530	
	I_{IL}	$V_{IN} = V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$	R_T = 50Ω, V_{TT} = −2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$	R_T = 50Ω, V_{TT} = −2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	Fig. 1	CP to Q	0.90	1.64	2.50	ns
			CP to $\overline{TC}$	1.70	3.10	4.70	
			MR to Q	1.30	2.00	2.65	
			MR to $\overline{TC}$	1.80	3.50	5.35	
			$D_0/\overline{CET}$ to $\overline{TC}$	1.50	2.60	4.00	
			Sn to $\overline{TC}$	1.00	2.25	3.25	
Transition Time	t_{TLH} t_{THL}			0.30	0.90	1.70	ns
Set-up Time	t_{su}	Fig. 2	Dn input	1.30	—	—	ns
			Pn input	1.60	—	—	
			$D_0/\overline{CET}$, CEP input	1.55	—	—	
			Sn input	3.55	—	—	
			MR input (Release Time)	2.70	—	—	
Hold Time	t_h		Dn input	−0.10	—	—	ns
			Pn input	−0.25	—	—	
			$D_0/\overline{CET}$, CEP input	−0.15	—	—	
			Sn input	−0.80	—	—	
Toggle Frequency	f_{tog}	See test circuit and waveform		300	—	—	MHz
Pulse Width	t_{pw}		CP(High)	1.70	—	—	ns
			MR(High)	2.20	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

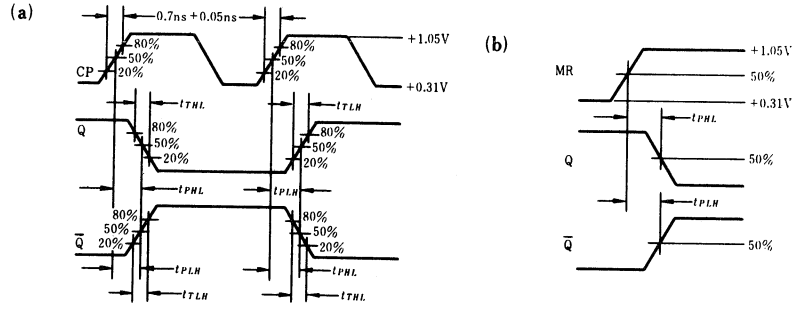


Fig.1 Propagation Delay Time

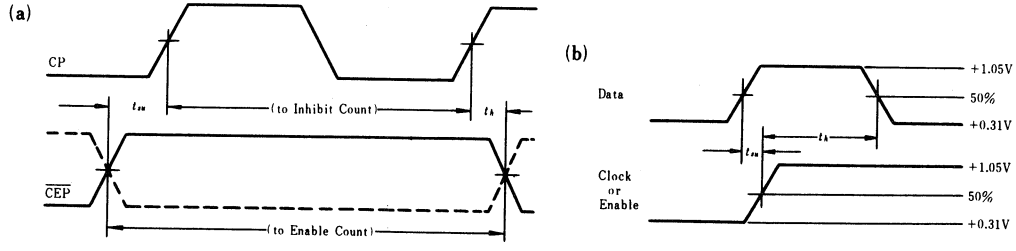
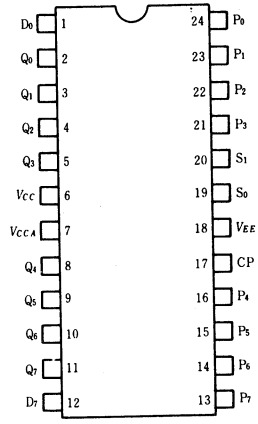


Fig.2 Set-up and Hold Time

8-bit Shift Registers

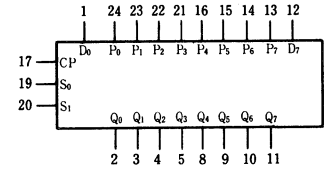
The HD100141 contains eight clocked D-type flip flops with individual inputs (Pn) and outputs (Qn) for parallel operation, and with serial inputs (Dn) and steering logic for bidirectional shifting.
The flip flops accept input data a set-up time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.
The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Function Sheet Table.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC SYMBOL



■ FUNCTION SHEET TABLE

Function	Input					Output							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↑	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↑	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↑	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	← No Change →							
Hold	X	X	X	X	H	← No Change →							
Hold	X	X	X	X	L	← No Change →							

H = High Level
L = Low Level
X = Don't Care
↑ = Low to High transition

DC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND, Ta=0∼+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		119	170	238	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	CP input	—	—	640	μA
			Other input	—	—	220	
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	R_T=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	R_T=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PHL} t_{PLH}	Fig. 1		1.05	1.70	2.40	ns
Transition Time	t_{TLH} t_{THL}			0.35	0.95	1.40	ns
Shift Frequency	f_{shift}			380	500	—	MHz
Set-up Time	t_{su}	Fig. 2	Serial-in, Parallel-in	0.95	—	—	ns
			Select input	2.00	—	—	
Hold Time	t_h		Serial-in, Parallel-in	0.20	—	—	ns
			Select input	−0.20	—	—	
Pulse Width	t_{pw}		CP	0.95	—	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

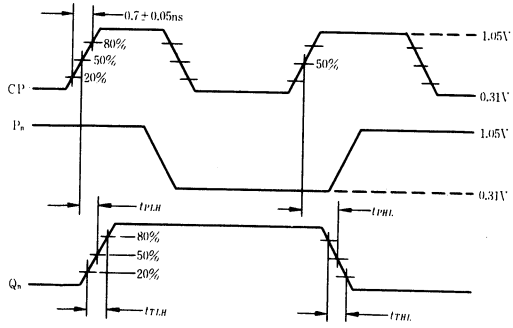


Fig.1 Propagation Delay Time

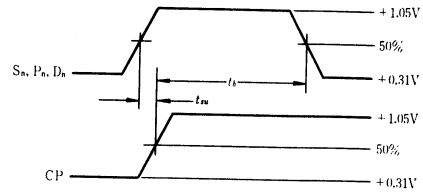
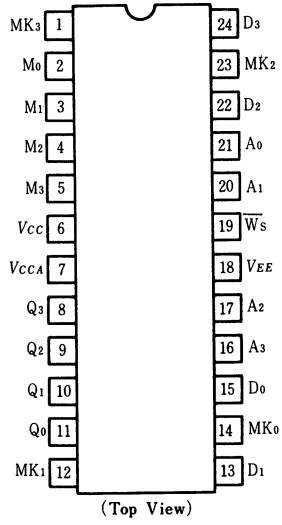


Fig.2 Set-up and Hold Time

4×4 Content Addressable Memory

The HD100142 is a 4 word x 4 bit Content Addressable Memory (CAM). Each word location has its own Address Select line. Reading or Writing is accomplished when the Address Select line is low. In the Read mode, Data from the addressed location appears at the Data (Qi) outputs.
In the Write mode, Data is stored in the addressed location. A low Write Strobe selects the Write mode, a high Write Strobe select the Read mode. Each Data input has its own Mask input that blocks data storage when the Mask is high. The Data input word is simultaneously compared with each of the four memory Words.
If a Search Compare result in a Match, this output will go low. A high Mask input on any bit forces a Match of that bit. Each input has a 50kΩ (typical) pull-down resistor tied to V_{EE}. The outputs require external resistance terminations as they are not terminated internally through resistance to the V_{EE} supply.

■ PIN ARRANGEMENT



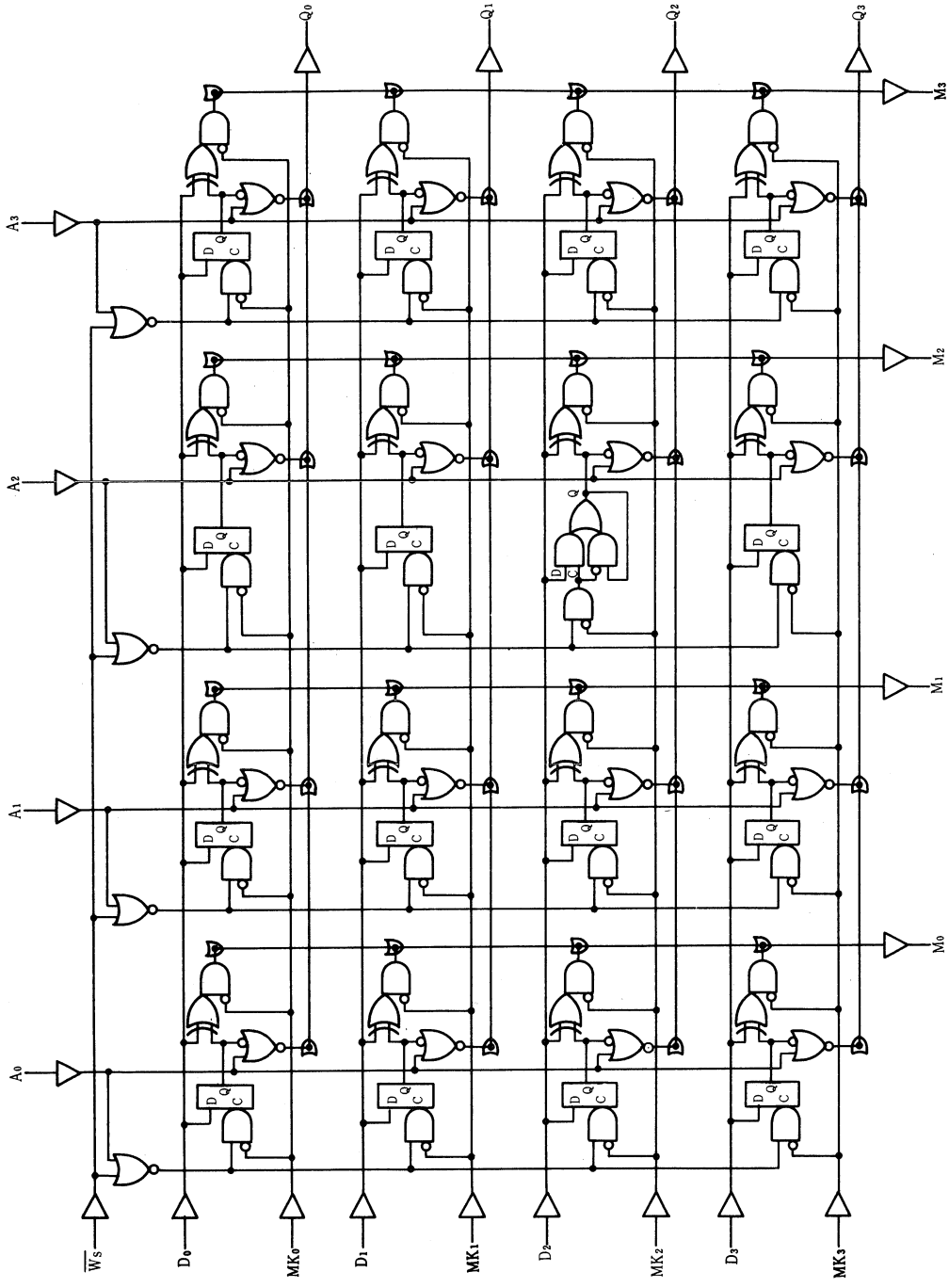
(Top View)

■ TRUTH TABLE

Operation	Inputs				Flip-Flop	Outputs	
	$\overline{WS}$	A_i	D_j	MK_j	Q_{ij}	M_i	Q_i
	$\overline{WS}$	A_0	D_0	MK_0		M_0	Q_0
		A_1	D_1	MK_1		M_1	Q_1
		A_2	D_2	MK_2		M_2	Q_2
		A_3	D_3	MK_3		M_3	Q_3
Write Disabled	×	H	×	×	NC	×	L
	×	L	×	H	NC	L	Q_{ijn-1}
	H	L	×	×	NC	×	Q_{ijn-1}
Write	L	L	H	L	H	L	H
	L	L	L	L	L	L	L
Read	H	L	×	×	H	×	H
	H	L	×	×	L	×	L
Match Masked	H	×	×	H	NC	L	×
Match Not Satisfied	H	L	H	L	L	H	L
	H	H	H	L	L	H	L
	H	H	L	L	H	H	L
	H	L	L	L	H	H	H
Match Satisfied	H	L	H	L	H	L	H
	H	H	H	L	H	L	L
	H	H	L	L	L	L	L
	H	L	L	L	L	L	L

H = High Voltage Level (Most Positive)
L = Low Voltage Level (Most Negative)
× = Don't Care (May be either high or low)
NC = No Change from Previous State
$\overline{WS}$ = Write Strobe
Ai = Address for ith Word
Dj = Data for jth Bit
MKj = Data mask for jth Bit (H = Mask)
Qij = Cell State for ith Word, jth Bit
Mi = Match Output of ith Word (L = True)
Qj = Data Output of jth Bit
Q_{n+1} = Previous Cell State

LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND, Ta=0∼+85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			114	163	288	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	$\overline{WS}$, Aj input		—	—	159	μA
			Dn input		—	—	149	
			MKn input		—	—	164	
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		R_T=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}				−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		R_T=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}				—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Address to Data Out	t_{AD}	Fig. 2, 3	1.30	1.90	2.90	ns
Data In to Match Out Time	t_{DM}	Fig. 4	1.35	2.45	3.55	
Mask In to "Enable Partial" Match Out Time	t_{MM}		1.25	1.95	2.85	
Data In to New Data Out	t_{DD}	Fig. 2	1.90	3.00	4.45	
Write to New Data Out	t_{WD}		2.20	3.40	4.60	
Address to Match	t_{AM}		2.20	3.45	4.70	
Mask to Data	t_{MD}		2.10	3.30	4.45	
$\overline{WS}$ to Match	t_{WSM}		2.20	3.30	4.60	
Write Pulse Width	t_W	Fig. 1 t_W=1.20ns	1.40	—	—	
Address Set-up Before Write Time	t_{AS}		0.20	—	—	
Address Hold After Write Time	t_{AH}		0.20	—	—	
Data In Set-up Before Write Time	t_{DS}		−0.60	—	—	
Data In Hold After Write Time	t_{DH}		0.70	—	—	
Mask In Hold to Inhibit Write Time	t_{MH}		1.30	—	—	
Mask In Set-up to Inhibit Write Time	t_{MS}		−0.20	—	—	
Transition Time	t_{TLH}		0.50	—	2.00	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

■ TIMING RELATION SHIPS (t_W=1.20ns)

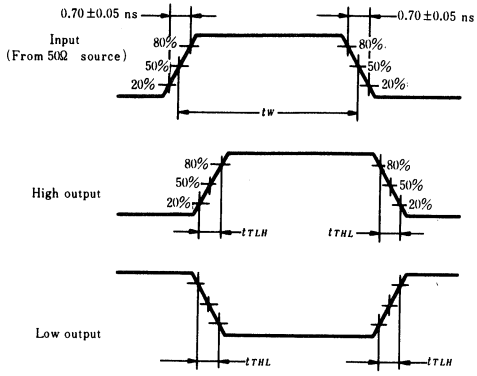


Fig.1 Output Rise and Fall Times and Waveforms

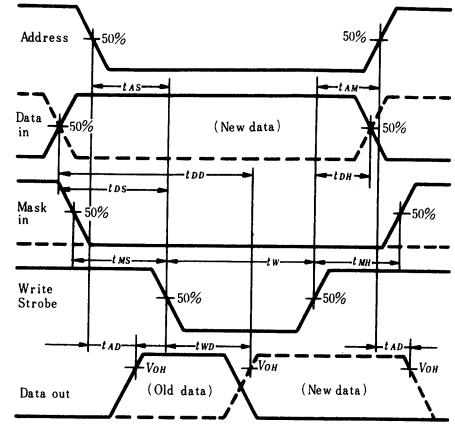


Fig.2 Write Mode and Read/Write Mode Waveforms

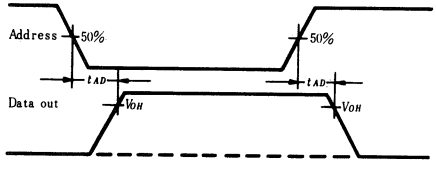


Fig.3 Read Mode Waveforms

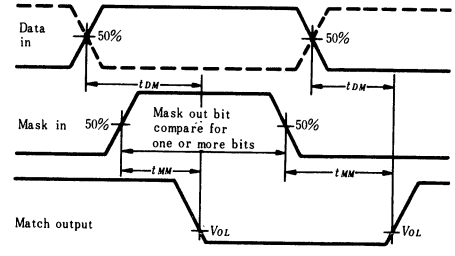


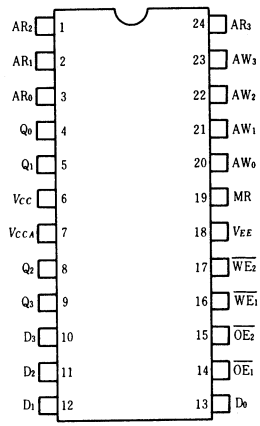
Fig.4 Search Mode Waveforms

HD100145

16×4 Read/Write Register File

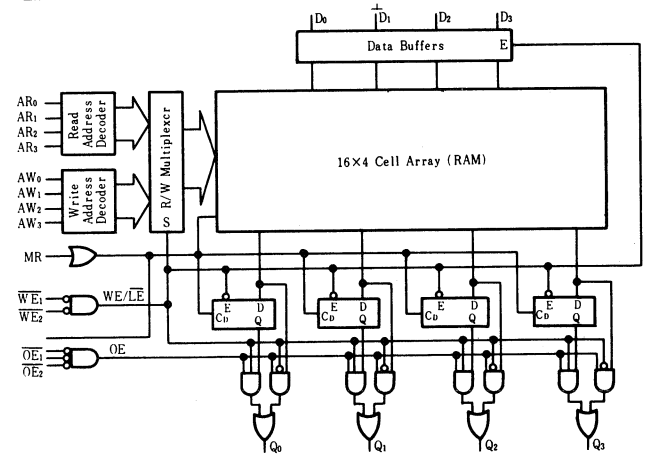
The HD100145 is a 64-bit Register File organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting-up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the WRITE mode and the latches are in a HOLD mode. When either $\overline{WE}$ input is HIGH, the circuit is in the READ mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches and forces the outputs LOW.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0~+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		119	170	247	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	WE/$\overline{LE}$ input	—	—	270	μA
			All input except WE/$\overline{LE}$	—	—	220	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IL\ min}$	R_L=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	R_L=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

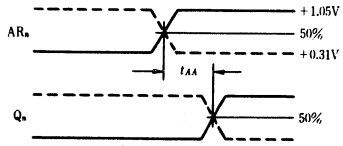
■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item		Symbol	Test Condition	min	typ	max	Unit
Access/ Recovery Timing	Address Access	t_{AA}	Fig. 1 a	2.00	5.50	7.40	ns
	Output Recovery	t_{OR}	Fig. 1 b	0.80	2.20	3.10	ns
	Output Disable	t_{OD}		0.80	2.20	3.10	ns
Read Timing	Address Set-up	t_{RSA1}	Fig. 1 c	3.20	2.00	—	ns
	Output Delay	t_{WEQ}		6.10	4.50	2.00	ns
Output Latch Timing	Address Set-up	t_{RSA2}	Fig. 1 d	8.50	5.50	—	ns
	Address Hold	t_{RHA}	Fig. 1 e	0.20	−2.00	—	ns
Write Timing	Address Set-up	t_{WSA}	Fig. 2 a	3.20	2.00	—	ns
	Address Hold	t_{WHA}		0.20	−1.30	—	ns
	Data Set-up	t_{WSD}		9.20	6.00	—	ns
	Data Hold	t_{WHD}		0.20	−1.20	—	ns
	Min. Write Pulse Width	t_W		6.20	4.00	—	ns
	$\overline{WE}$ to $\overline{WE}$ Set-up	t_{SW}	Fig. 2 b	0.70	—	—	ns
	$\overline{WE}$ to $\overline{WE}$ Hold	t_{HW}		0.20	—	—	ns
Master Reset Timing	Min. Reset Pulse Width	t_M	Fig. 3 a	4.50	—	—	ns
	$\overline{WE}$ Hold to Write	t_{MHW}		7.20	—	—	ns
	Output Disable	t_{MQ}	Fig. 3 b	3.70	2.70	—	ns

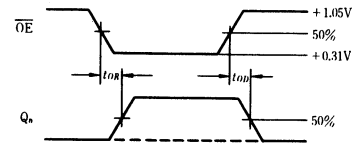
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

■ TIMING RELATIONSHIPS

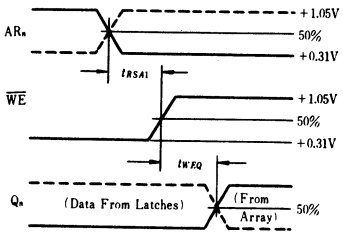
(a) Address Access Time
($\overline{WE}_1$, or $\overline{WE}_2$ = High : $\overline{OE}_1$ = $\overline{OE}_2$ = Low)



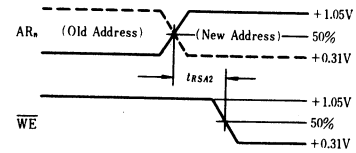
(b) Output Recovery/Disable Time
(unpulsed $\overline{OE}$ = Low)



(c) Read Timing, Address Set-up Time
(unpulsed $\overline{WE}$, $\overline{OE}_1$, $\overline{OE}_2$ = Low)



(d) Output Latch Timing, Address Set-up Time
(unpulsed $\overline{WE}$ = Low)



(e) Output Latch Timing, Address Hold Time
(unpulsed $\overline{WE}$ = Low)

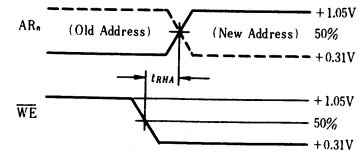
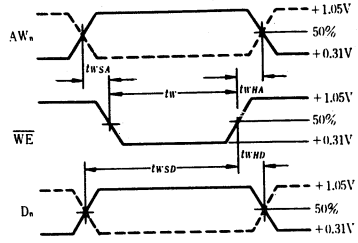


Fig. 1 Read Timing

(a) Address and Data Set-up Time and Hold Time, Write Pulse Width (unpulsed $\overline{WE}$=Low)



(b) $\overline{WE}$ Set-up and hold times, write with other $\overline{WE}$

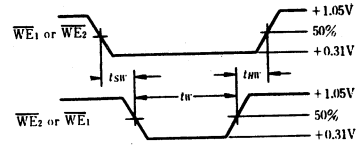
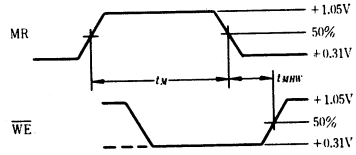


Fig.2 Write Timing

(a) Reset pulse width, $\overline{WE}$ hold time for subsequent writing (address already set-up, unpulsed $\overline{WE}$=Low)



(b) Output reset delay, MR to Q_n

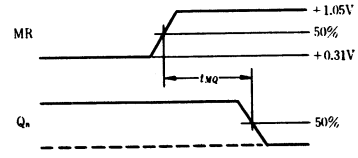
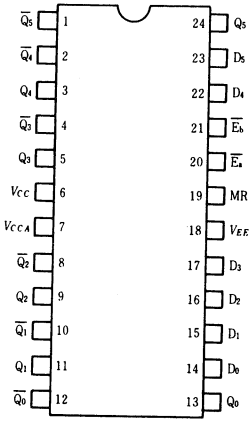


Fig.3 Master Reset Timing

Hex D-type Latches

The HD100150 contains six D type latches with the True and Complement Outputs, a pair of Common Enables ($\overline{Ea}$ and $\overline{Eb}$), and a common Master Reset(MR). A Q output follows its D input when both $\overline{Ea}$ and $\overline{Eb}$ are low. When either $\overline{Ea}$ or $\overline{Eb}$ (or both) are high, a latch stores the last valid data present on its D input before $\overline{Ea}$ or $\overline{Eb}$ went high. The MR input overrides all other inputs and makes the Q outputs low.

■ PIN ARRANGEMENT



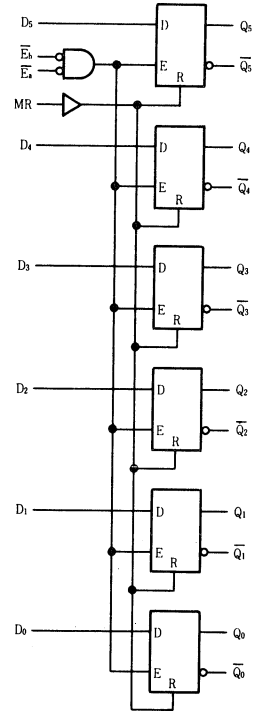
(Top View)

■ TRUTH TABLE (each latch)

Dn	$\overline{Ea}$	$\overline{Eb}$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
×	H	×	L	*
×	×	H	L	*
×	×	×	H	L

H = High Level
L = Low Level
× = Immaterial
* = Retains data present before $\overline{E}$ positive transition

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			79	113	159	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	MR input		—	—	450	μA
			Data input		—	—	340	μA
			Enable input		—	—	520	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IL}=V_{IL\ min}$		R_L=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}				−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		R_L=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}				—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	Fig. 1	Enable input	0.75	1.15	1.70	ns
			MR input ($\overline{Ea}$=$\overline{Eb}$=L)	1.10	1.85	2.55	
			Data input	0.55	0.85	1.60	
Transition Time	t_{TLH} t_{THL}			0.35	0.90	1.50	ns
Set-up Time	t_{su}	Fig. 2	Data input	0.80	—	—	ns
			MR input (Release Time)	2.20	—	—	
Hold Time	t_h		Data input	0.50	—	—	ns
Pulse Width	t_{PW}		$\overline{E}$ (Low)	0.95	—	—	ns
			MR (High)	1.50	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

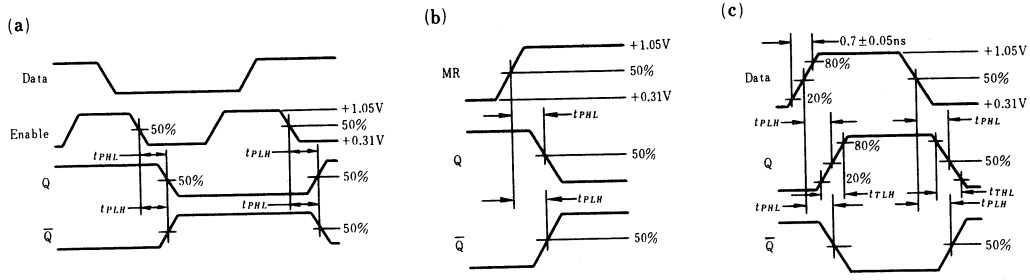


Fig. 1 Propagation Delay Time

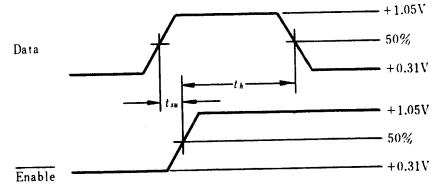


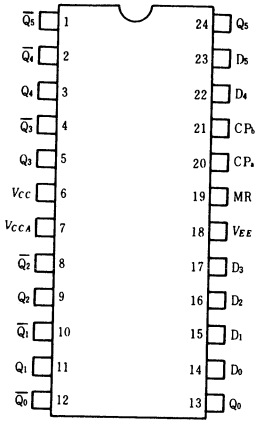
Fig. 2 Set-up and Hold Time

HD100151

Hex D-type Flip-Flops

HD100151 contains six master/slave fli-flops with True and Complement outputs. A pair of Common Clock inputs (CPa and CPb) and common Master Reset (MR) input. Data enters a master when both CPa and CPb are low and transfers to the slave when CPa or CPb (or both) go high. The MR inputs overrides all other inputs and makes the Q outputs low.

■ PIN ARRANGEMENT



(Top View)

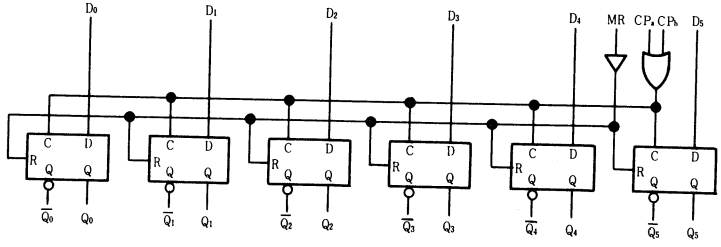
■ TRUTH TABLE (Each Flip Flop)

D_n	CP_a	CP_b	MR	$Q_{n(t+1)}$
L	⎍	L	L	L
H	⎍	L	L	H
L	L	⎍	L	L
H	L	⎍	L	H
×	H	⎍	L	$Q_{n(t)}$
×	⎍	H	L	$Q_{n(t)}$
×	×	×	H	L

×: Immaterial

t, t+1 : Time before and after CP positive transition

■ LOGIC DIAGAM



■ DC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND, Ta=0~+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		98	141	198	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	MR input	—	—	450	μA
			D_0~D_5 input	—	—	225	
			CP_a, CP_b input	—	—	520	
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	R_T=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	R_T=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See Test Circuit and Waveform	CP input	0.80	1.30	1.90	ns
			MR input	1.20	1.85	2.60	
Transition Time	t_{TLH} t_{THL}			0.30	0.90	1.20	ns
Toggle Frequency	f_{Tog}			400	550	—	MHz
Set-up Time	t_{su}		D input	0.80	—	—	ns
			MR input (Release Time)	2.20	—	—	
Hold Time	t_h		D input	0.50	—	—	
Pulse Width	t_{PW}		CP (High)	1.30	—	—	ns
			MR (High)	1.50	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Quad. Multiplexers/Latches

The HD100155 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{En}$) inputs are low, the data that appears at an outputs is controlled by the Select (Sn) inputs, as shown in the operating mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs low for the case where the latch is transparent (both Enables are low) and can steer a high signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1.

A positive-going signal on either Enable input latches the outputs. A high signal on the Master Reset (MS) input overrides all the other inputs and forces the Q outputs low.

■ OPERATING MODE TABLE

CONTROLS				OUTPUT
$\overline{E_1}$	$\overline{E_2}$	$\overline{S_0}$	S_1	Q_n
H	×	×	×	latched*
×	H	×	×	latched*
L	L	L	L	D_{0n}
L	L	L	H	$D_{0n}+D_{1n}$
L	L	H	L	L
L	L	H	H	D_{1n}

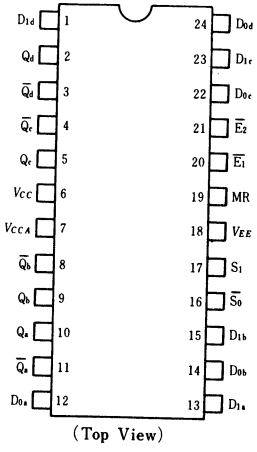
H = High Level
L = Low Level
× = Immaterial
* = Stores data present before $\overline{En}$ went high.

■ TRUTH TABLE

Input							Output	
MR	$\overline{E_1}$	$\overline{E_2}$	S_1	$\overline{S_0}$	D_{1a} D_{1b} D_{1c} D_{1d}	D_{0a} D_{0b} D_{0c} D_{0d}	$\overline{Q_a}$ $\overline{Q_b}$ $\overline{Q_c}$ $\overline{Q_d}$	Q_a Q_b Q_c Q_d
H	×	×	×	×	×	×	H	L
L	L	L	H	H	H	×	L	H
L	L	L	H	H	L	×	H	L
L	L	L	L	L	×	H	L	H
L	L	L	L	L	×	L	H	L
L	L	L	L	H	×	×	H	L
L	L	L	H	L	H	×	L	H
L	L	L	H	L	×	H	L	H
L	L	L	H	L	L	L	H	L
L	H	×	×	×	×	×	No Change	
L	×	H	×	×	×	×	No Change	

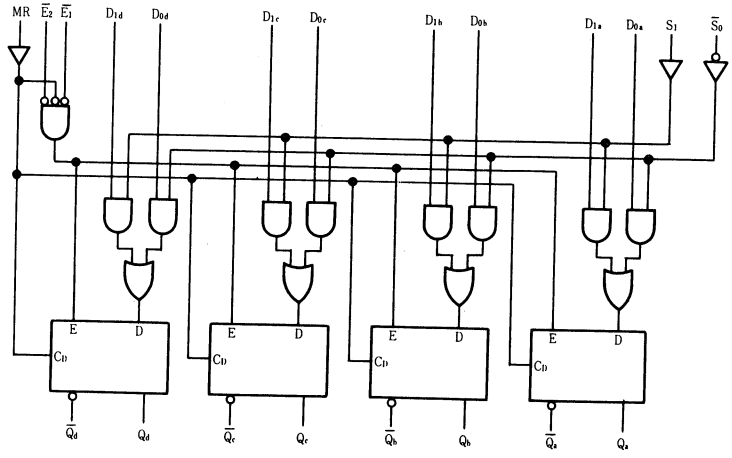
H = High Level
L = Low Level
× = Immaterial

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND, Ta=0~+85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			66	95	133	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	S_n input		—	—	220	μA
			$\overline{E_n}$ input		—	—	350	
			Data input		—	—	340	
			MR input		—	—	430	
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		R_T=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}				−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		R_T=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}				—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

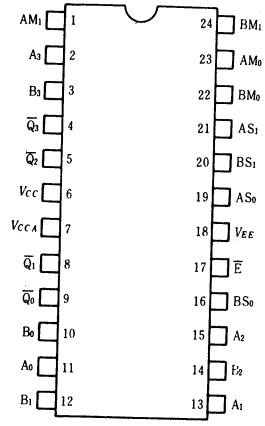
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See Test Circuit and Waveform	Data input	0.50	1.20	1.75	ns
			S input	1.30	2.50	3.45	
			$\overline{E}$ input	0.80	1.70	2.40	
			MR input	0.80	1.85	2.90	
Transition Time	t_{TLH} t_{THL}			0.35	1.10	1.65	ns
Set-up Time	t_{su}		Data input	0.60	—	—	ns
			S input	2.30	—	—	
			MR input (Release Time)	1.60	—	—	
Hold Time	t_h		Data input	0.30	—	—	ns
			S input	−0.50	—	—	
Pulse Width	t_{pw}		$\overline{E_1}$, $\overline{E_2}$ (Low)	1.60	—	—	ns
			MR (High)	1.45	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Mask-merge

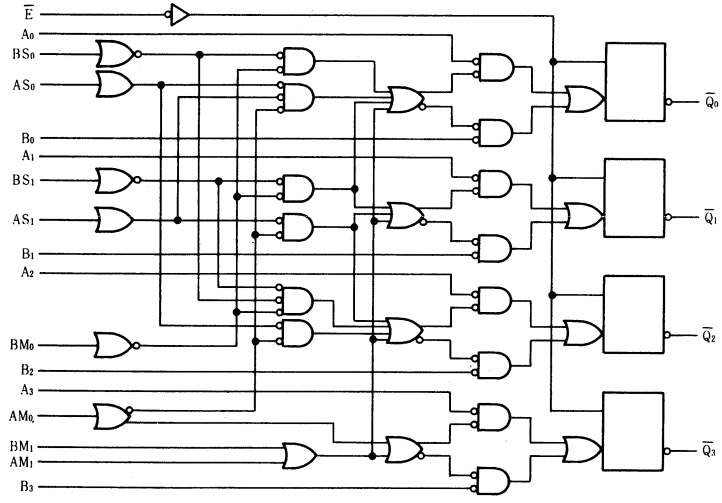
The HD100156 merges two 4-bit words to form a 4-bit output word. The AMj enable allows the merge of An into Bn by one, two, or three places (per the ASj value) from the left. The BMj enable similarly allows the merge of Bn into An from the left (per the BSj value). The Bn merge overrides the An merge when both are enabled. This means An first merges into Bn and Bn then merges into the An merge. A Bn address (BSj) greater than or equal to the An address (ASj) thus forces the outputs to all Bn. The merge outputs feed 4 latches, which have a common enable ($\overline{E}$) input. All inputs have a 50kΩ (typ.) pull-down resistor tied to V_{EE}.
All four outputs do not have pull-down resistors, so they have wired-OR capability and will require external resistors.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Input									Output				
BM_1	BM_0	AM_1	AM_0	BS_1	BS_0	AS_1	AS_0	$\overline{E}$	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	
×	×	H	×	×	×	×	×	L	B_0	B_1	B_2	B_3	
H	×	×	×	×	×	×	×	L	B_0	B_1	B_2	B_3	
L	L	L	L	×	×	×	×	L	A_0	A_1	A_2	A_3	
L	L	L	H	×	×	L	L	L	B_0	B_1	B_2	B_3	
L	L	L	H	×	×	L	H	L	A_0	B_1	B_2	B_3	
L	L	L	H	×	×	H	L	L	A_0	A_1	B_2	B_3	
L	L	L	H	×	×	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	×	×	L	A_0	A_1	A_2	A_3	
L	H	L	L	L	H	×	×	L	B_0	A_1	A_2	A_3	
L	H	L	L	H	L	×	×	L	B_0	B_1	A_2	A_3	
L	H	L	L	H	H	×	×	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	L	L	B_0	A_1	B_2	B_3	
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	B_3	
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	ADDRESS (BS) > ADDRESS (AS)
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
×	×	×	×	×	×	×	×	H	Q_0	Q_1	Q_2	Q_3	

H = High Level
L = Low Level
× = Don't Care

■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			107	153	214	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	BS_j, AS_j, $\overline{E}$, BM_j, AM_j		—	—	265	μA
			A_n, B_n		—	—	340	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$		R_T = 50Ω, V_{TT} = −2.0V	−1025	−955	−880	mV
	V_{OL}				−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$		R_T = 50Ω, V_{TT} = −2.0V	−1035	—	—	mV
	V_{OLC}				—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See Test Circuit and Waveforms	A_n, B_n	0.70	1.20	1.85	ns
			$\overline{E}$	1.40	2.00	3.00	
			Address	1.60	2.60	3.75	
			AM_j, BM_j	1.60	2.70	4.05	
Transition Time	t_{TLH} t_{THL}			0.50	0.90	3.00	ns
Set-up Time	t_{su}		Data	0.20	—	—	ns
			AM_j, BM_j	2.00	—	—	
			AS_j, BS_j	2.00	—	—	
Hold Time	t_h		Data	1.70	—	—	ns
			AM_j, BM_j	−0.30	—	—	
			AS_j, BS_j	−0.30	—	—	
Pulse Width	t_{PW}		$\overline{E}$ (Low)	1.60	—	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

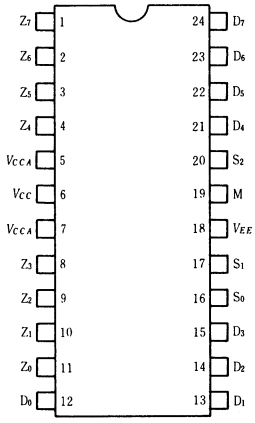
8-bit Shift Matrix

The HD100158 contains a combinatorial network which performs the function of an 8-bit shift matrix. Three control lines (Sn) are internally decoded and define the number of places which an 8-bit word present at the inputs (Dn) is shifted to the left and presented at the outputs (Zn). A Mode Control input (M) is provided which if low, forces low all outputs to the right of the one that contain D_7. This operation is sometimes referred to as "low backfill".

If M is high, an end-round shift is performed such that D_0 appears at the output to the right of the one that contains D_7.

This operation is commonly referred to as "barrel shifting".

■ PIN ARRANGEMENT



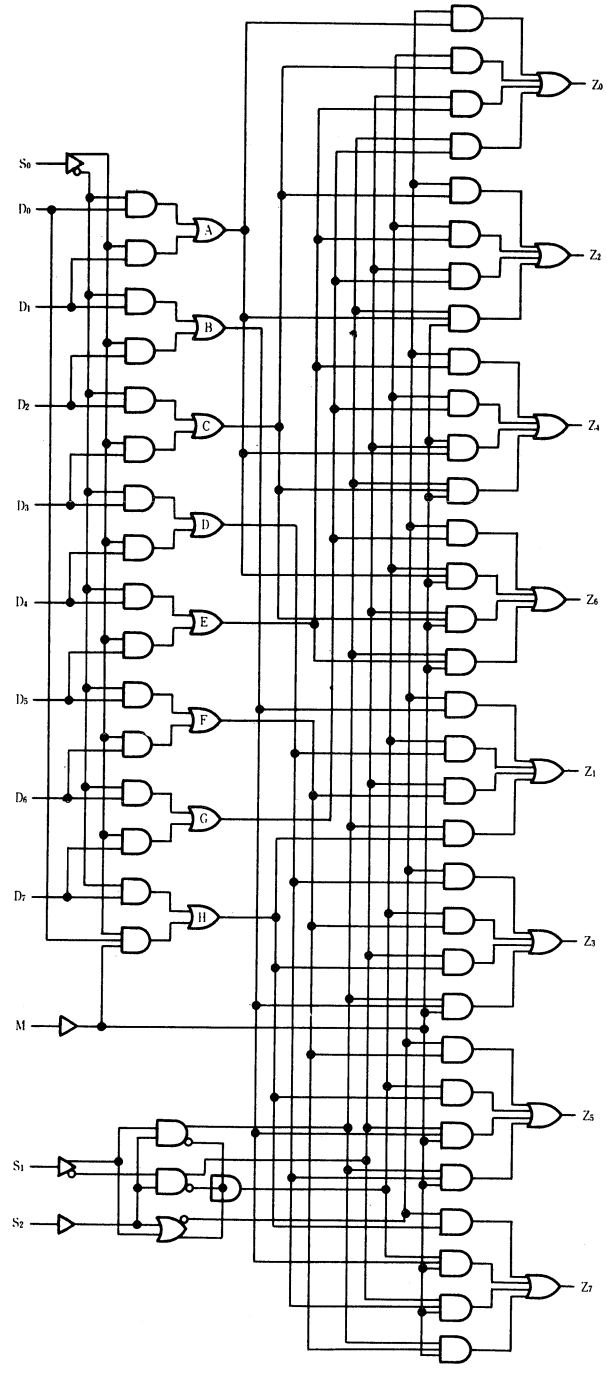
(Top View)

■ TRUTH TABLE

INPUT				OUTPUT							
M	S_0	S_1	S_2	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
×	L	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
L	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L
L	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	L	L
L	H	H	L	D_3	D_4	D_5	D_6	D_7	L	L	L
L	L	L	H	D_4	D_5	D_6	D_7	L	L	L	L
L	H	L	H	D_5	D_6	D_7	L	L	L	L	L
L	L	H	H	D_6	D_7	L	L	L	L	L	L
L	H	H	H	D_7	L	L	L	L	L	L	L
H	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0
H	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1
H	H	H	L	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2
H	L	L	H	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3
H	H	L	H	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4
H	L	H	H	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5
H	H	H	H	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6

H = High level
L = Low level
× = Immaterial

LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		84	120	168	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$		—	—	220	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$	R_T = 50Ω	−1025	−955	−880	mV
	V_{OL}		V_{TT} = −2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$	R_T = 50Ω	−1035	—	—	mV
	V_{OLC}		V_{TT} = −2.0V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	D input	1.00	1.70	2.45	ns
			M input	1.25	2.30	3.90	
			S_n input	1.50	2.30	3.75	
Transition Time	t_{TLH} t_{THL}			0.50	1.30	2.20	ns

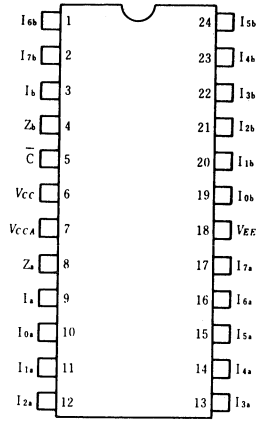
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100160

Dual Parity Generators/Checkers

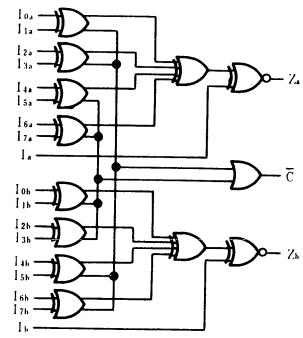
The HD100160 is a Dual Parity Checker/Generator. Each half has nine inputs, with the output being high when an even number of inputs are high. One of the nine inputs(Ia or Ib) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits. The HD100160 also has a Compare ($\overline{C}$) output which allows the circuit to compare two 8-bit words.
The $\overline{C}$ output is low when the two words match, bit for bit.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE (each half)

Sum of High Input	Output Z
EVEN	H
ODD	L

$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$

■ DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		57	82	115	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	Ib, Ia	—	—	340	μA
			All input except Ib and Ia	—	—	220	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}		$V_{TT}=-2.0V$	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS ($V_{EE}=-2.5V$, $V_{CC}=2.0V$, $Ta=25°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	Ina, Inb to Z	1.30	2.50	3.80	ns
			Ina, Inb to $\overline{C}$	1.20	2.00	2.95	ns
			Ia, Ib to Z	0.60	0.90	1.25	ns
Transition Time	t_{TLH} t_{THL}			0.40	0.90	1.40	ns

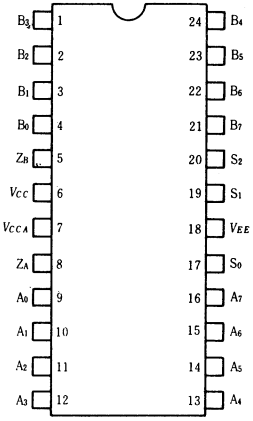
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100163

Dual 8-input Multiplexers

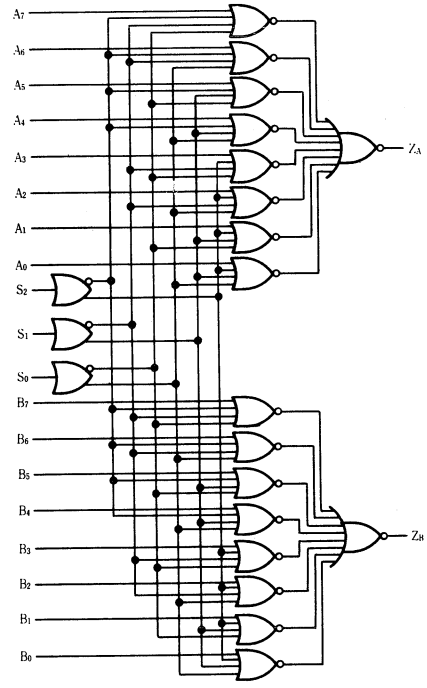
The HD100163 is a dual 8-input Multiplexer. The Data Select(Sn) inputs determine which bit (An and Bn) will be presented at the Outputs (Z_A and Z_B respectively). The same bit (0–7) will be selected for both the Z_A and Z_B output.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Input										Output
Address			Data							
S_2	S_1	S_0	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	
L L	L L	L L	×	×	×	×	×	×	×	L H	L H
L L	L L	H H	×	×	×	×	×	×	L H	×	L H
L L	H H	L L	×	×	×	×	×	L H	×	×	L H
L L	H H	H H	×	×	×	×	L H	×	×	×	L H
H H	L L	L L	×	×	×	L H	×	×	×	×	L H
H H	L L	H H	×	×	L H	×	×	×	×	×	L H
H H	H H	L L	×	L H	×	×	×	×	×	×	L H
H H	H H	H H	L H	×	×	×	×	×	×	×	L H

■ DC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND, Ta=0～+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		76	109	153	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	S_n input	—	—	265	μA
			A_n, B_n input	—	—	340	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	R_L=50Ω	−1025	−955	−880	mV
	V_{OL}		V_{TT}=−2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	R_L=50Ω	−1035	—	—	mV
	V_{OLC}		V_{TT}=−2.0V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveforms	Data input	0.60	0.95	1.60	ns
	t_{PHL}		Select input	1.10	1.75	2.50	
Transition Time	t_{TLH}			0.55	1.20	1.70	ns
	t_{THL}						

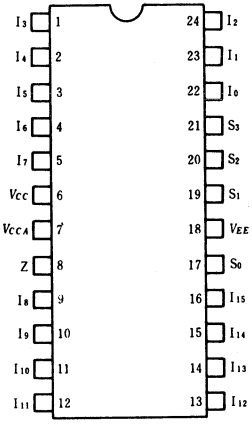
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100164

16-input Multipiexers

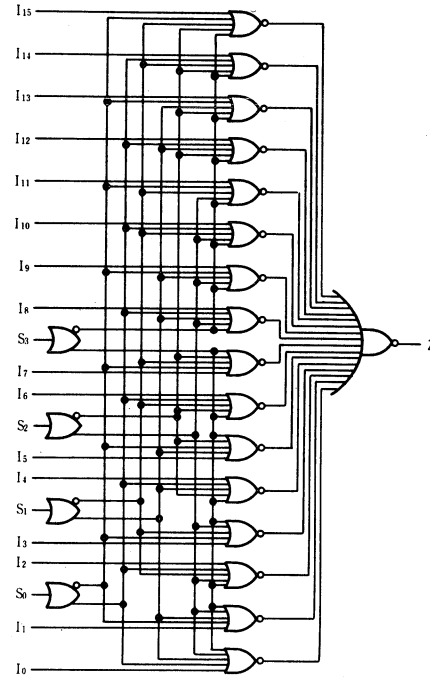
The HD100164 is a 16-input Multiplexer. Data paths are controlled by four select line (S_0–S_3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		43	70	98	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	In input	—	—	280	μA
			S_0, S_1 input	—	—	240	μA
			S_2, S_3 input	—	—	200	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	R_L=50Ω	−1025	−955	−880	mV
	V_{OL}		V_{TT}=−2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IN\ min}$ or $V_{IN}=V_{IL\ max}$	R_L=50Ω	−1035	—	—	mV
	V_{OLC}		V_{TT}=−2.0V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	In input	0.95	1.60	2.75	ns
			S_0, S_1 input	1.45	2.40	3.55	
			S_2, S_3 input	1.10	1.85	2.95	
Transition Time	t_{TLH} t_{THL}			0.60	1.00	1.60	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100165

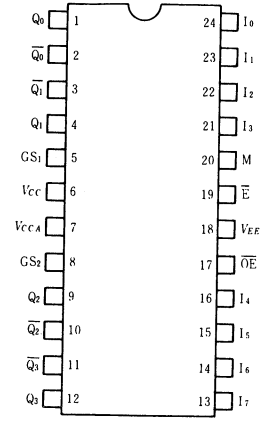
Universal Priority Encoders

The HD100165 contains eight input latches with a Common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a high signal. The circuit operates as a dual 4-input encoder when the Mode Control input (M) is low, and as a single 8-input encoder when M is high.

In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with I_0-I_3. Q_2, Q_3 and GS_2 operate with I_4-I_7.

A GS output goes low when its pertinent inputs are all low. Inputs are latched when $\overline{E}$ goes high. A high signal on the Output Enable ($\overline{OE}$) input forces all Q outputs low and GS outputs high. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group.

■ PIN ARRANGEMENT



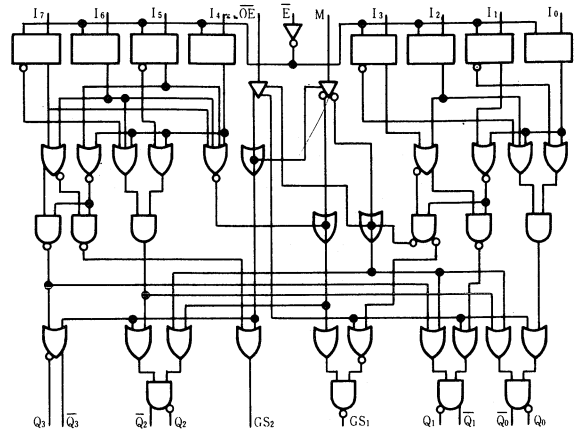
(Top View)

■ TRUTH TABLE

$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	×	×	×					L	L			H	
L	L	L	L	H	×	×					H	L			H	
L	L	L	L	L	H	×					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	×	×	×			L	L		H
L	L	L					L	H	×	×			H	L		H
L	L	L					L	L	H	×			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	×	×	×	×	×	×	×	L	L	L	L	H	H
L	L	H	L	H	×	×	×	×	×	×	H	L	L	L	H	H
L	L	H	L	L	H	×	×	×	×	×	L	H	L	L	H	H
L	L	H	L	L	L	H	×	×	×	×	H	H	L	L	H	H
L	L	H	L	L	L	L	H	×	×	×	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	×	×	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	×	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
×	H	×	×	×	×	×	×	×	×	×	L	L	L	L	H	H
H	L	L	×	×	×	×	×	×	×	×	*	*	*	*	*	*
H	L	H	×	×	×	×	×	×	×	×	*	*	*	*	*	*

H = High Level
L = Low Level
* = Stores data present before $\overline{E}$ went high.

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND, Ta=0~+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		77	110	154	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$		—	—	230	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	R_T=50Ω,	−1025	−955	−880	mV
	V_{OL}		V_{TT}=−2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	R_T=50Ω,	−1035	—	—	mV
	V_{OLC}		V_{TT}=−2.0V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	Fig. 1	In→Qn, $\overline{Qn}$	1.10	2.15	3.40	ns
			In→GS1, GS2	1.00	2.00	3.40	
			$\overline{E}$→Qn, $\overline{Qn}$	1.40	3.00	4.00	
			$\overline{E}$→GS1, GS2	1.40	3.00	4.00	
			$\overline{OE}$→Qn, $\overline{Qn}$	1.00	1.75	2.60	
			$\overline{OE}$→GS1, GS2	1.00	1.80	2.85	
			M→Qn, $\overline{Qn}$	1.00	2.00	3.20	
			M→GS1, GS2	1.00	2.00	3.20	
Transition Time	t_{TLH} t_{THL}			0.30	0.90	1.30	ns
Set-up Time	t_{su}	Fig. 2	In input	0.80	—	—	ns
Hold Time	t_h			0.50	—	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

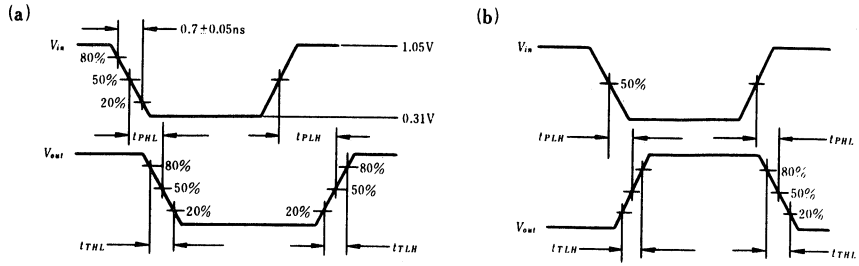


Fig.1 Propagation Delay Time

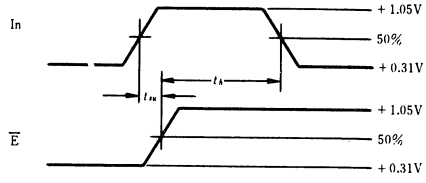
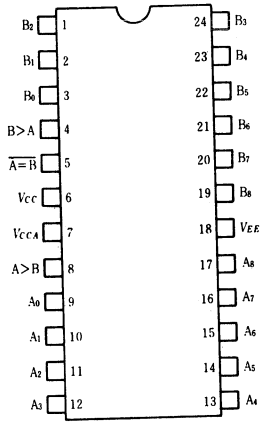


Fig.2 Set-up and Hold Time

9-bit Comparators

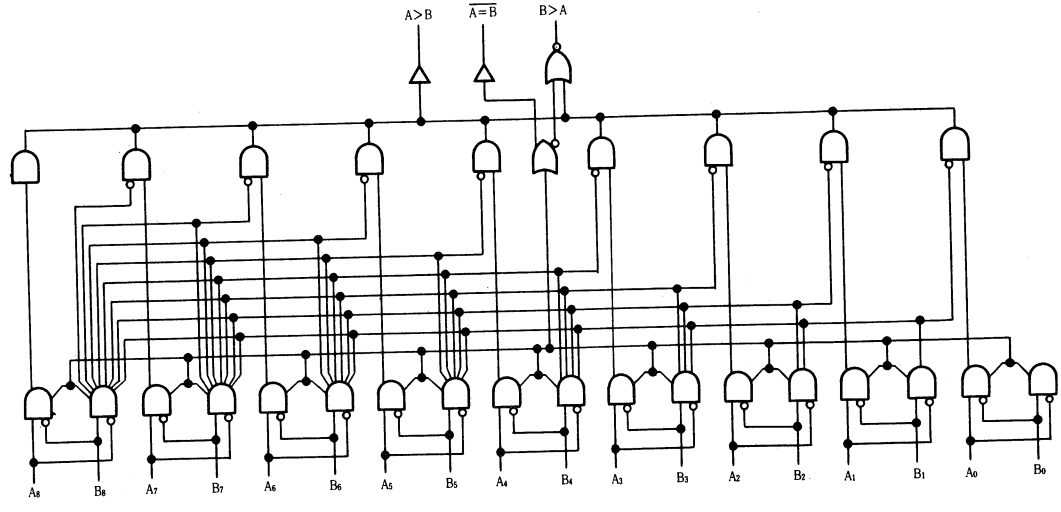
The HD100166 is a 9-bit Magnitude Comparator which compares the arithmetic value of two 9-bit words and indicates whether one word is greater than, or equal to the other.
The outputs do not have pull down resistors, which provides the wire OR functions by trying several outputs together.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



TRUTH TABLE

Input									Output		
A_8 B_8	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	A>B	B>A	$\overline{A=B}$
H L									H	L	H
L H									L	H	H
$A_8=B_8$	H L								H	L	H
$A_8=B_8$	L H								L	H	H
$A_8=B_8$	$A_7=B_7$	H L							H	L	H
$A_8=B_8$	$A_7=B_7$	L H							L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	H L						H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	L H						L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	H L					H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	L H					L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	H L				H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	L H				L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	H L			H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	L H			L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	H L		H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	L H		L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	H L	H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	L H	L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L

H = High Level
L = Low Level
Blank = Don't care

DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		119	170	238	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$		—	—	250	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_T=50\Omega$,	−1025	−955	−880	mV
	V_{OL}		$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_T=50\Omega$,	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	1.20	2.10	3.20	ns
	t_{PHL}					
Transition Time	t_{TLH}		0.45	0.90	1.35	ns
	t_{THL}					

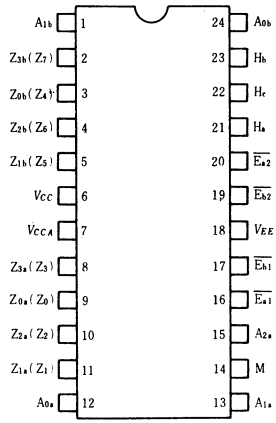
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Universal Demultiplexers/Decoders

The HD100170 Universal Demultiplexer/Decoder functions as either a dual Mode Control input(M). In the dual mode, each half has a pair of active low Enable($\overline{E}$) inputs. Pin assignments for the $\overline{E}$ inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active low enables (pin 16 to 17 and pin 19 to 20).

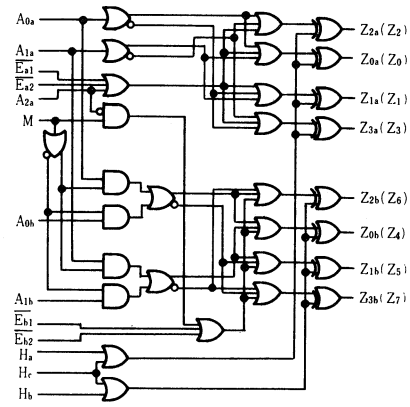
Signals applied to auxiliary inputs Ha, Hb and Hc determine whether the outputs are active high or active low. In the dual 1-of-4 mode the address inputs are A0a, A1a and A0b, A1b with A2a unused (i.e., left open, tied to V_{BB} or with low signal applied). In the 1-of-8 mode, the address inputs are A0a, A1a, A2a with A0b and A1b low or open.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



(Zn) for 1-of-8 applications

■ TRUTH TABLE

● Dual 1-of-4 Mode ($M = A_{2a} = Hc = L$)

Input				Active High Output ($H_a, H_b = H$)				Active Low Output ($H_a, H_b = L$)			
$\overline{E_{a1}}$	$\overline{E_{a2}}$	A_{1a}	A_{0a}	Z_{0a}	Z_{1a}	Z_{2a}	Z_{3a}	Z_{0a}	Z_{1a}	Z_{2a}	Z_{3a}
$\overline{E_{b1}}$	$\overline{E_{b2}}$	A_{1b}	A_{0b}	Z_{0b}	Z_{1b}	Z_{2b}	Z_{3b}	Z_{0b}	Z_{1b}	Z_{2b}	Z_{3b}
H	×	×	×	L	L	L	L	H	H	H	H
×	H	×	×	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

● Single 1-of-8 Mode ($M=H$: $A_{0b}=A_{1b}=H_a=H_b=L$)

Input					Active High Output ($H_C=H$)*							
$\overline{E_1}$	$\overline{E_2}$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	×	×	×	×	L	L	L	L	L	L	L	L
×	H	×	×	×	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

* For H_C = Low, output states are complemented.
$E_1=E_{a1}\cdot E_{b1}$, $E_{a2}\cdot E_{b2}$

■ DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		76	109	153	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	H_c, A_0, A_{1a}, A_{2a} input	—	—	310	μA
			All other input	—	—	250	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_L=50\Omega$, $V_{TT}=-2.0V$	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS ($V_{EE}=-2.5V$, $V_{CC}=2.0V$, $Ta=25°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	$\overline{E_a}/\overline{E_b}$ input	0.90	1.35	1.95	ns
			A input	0.90	1.60	2.40	ns
			H input	1.00	1.75	2.80	ns
			M input	1.55	2.60	3.70	ns
Transition Time	t_{TLH} t_{THL}			0.35	1.00	2.20	ns

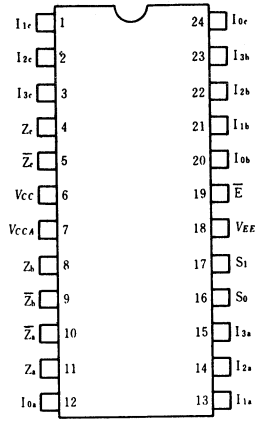
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100171

Triple 4-input Multiplexers with Enable

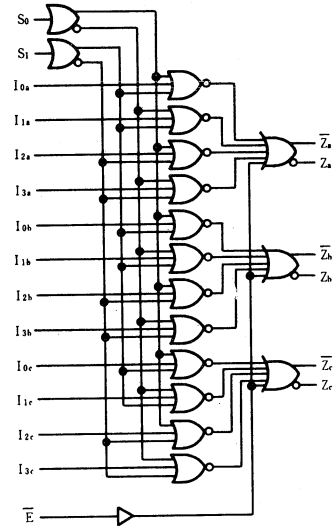
The HD100171 contains Triple 4-input multiplexers which share a common decoder (inputs S0 and S1). Output buffer gates provide true and complement outputs. A high on the Enable input ($\overline{E}$) forces all true outputs low (see truth table).

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0n}
L	H	L	I_{1n}
L	L	H	I_{2n}
L	H	H	I_{3n}
H	×	×	L

■ DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			56	81	114	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	S_0, S_1, $\overline{E}$ input		—	—	300	μA
			Data input		—	—	340	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}			$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}			$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$°C)

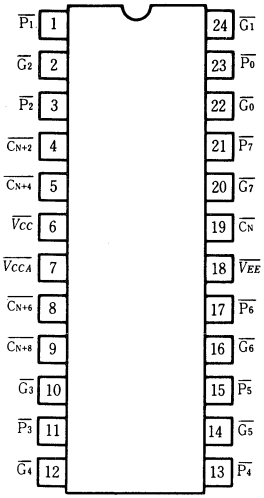
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	Data input	0.55	0.95	1.50	ns
			S_0/S_1 input	1.00	1.60	2.40	ns
			$\overline{E}$ input	0.90	1.50	2.25	ns
Transition Time	t_{TLH}, t_{THL}			0.40	0.90	1.40	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Carry Look-ahead

The HD100179 is a high speed carry look-ahead generator intended for use with the HD100180 6-bit fast Adder and the HD100181 4-bit ALU.

■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

● $\overline{C_{N+2}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{C_{N+2}}$
×	×	×	L	×	L
×	L	×	×	L	L
L	×	L	×	L	L
All other combinations					H

$\overline{C_{N+2}} = \overline{G_1} \cdot (\overline{P_1} + \overline{G_0}) \cdot (\overline{P_1} + \overline{P_0} + \overline{C_N})$

× = Don't care

● $\overline{C_{N+4}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	$\overline{C_{N+4}}$
×	×	×	×	×	×	×	L	×	L
×	×	×	×	×	L	×	×	L	L
×	×	×	L	×	×	L	×	L	L
×	L	×	×	L	×	L	×	L	L
L	×	L	×	L	×	L	×	L	L
All other combinations									H

$\overline{C_{N+4}} = \overline{G_3} \cdot (\overline{P_3} + \overline{G_2}) \cdot (\overline{P_3} + \overline{P_2} + \overline{G_1}) \cdot (\overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0}) \cdot (\overline{P_3} + \overline{P_2} + \overline{P_0} + \overline{C_N})$

● $\overline{C_{N+6}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	$\overline{G_4}$	$\overline{P_4}$	$\overline{G_5}$	$\overline{P_5}$	$\overline{C_{N+6}}$
×	×	×	×	×	×	×	×	×	×	×	L	×	L
×	×	×	×	×	×	×	×	×	L	×	×	L	L
×	×	×	×	×	×	×	L	×	×	L	×	L	L
×	×	×	×	×	L	×	×	L	×	L	×	L	L
×	×	×	L	×	×	L	×	L	×	L	×	L	L
×	L	×	×	L	×	L	×	L	×	L	×	L	L
L	×	L	×	L	×	L	×	L	×	L	×	L	L
All other combinations													H

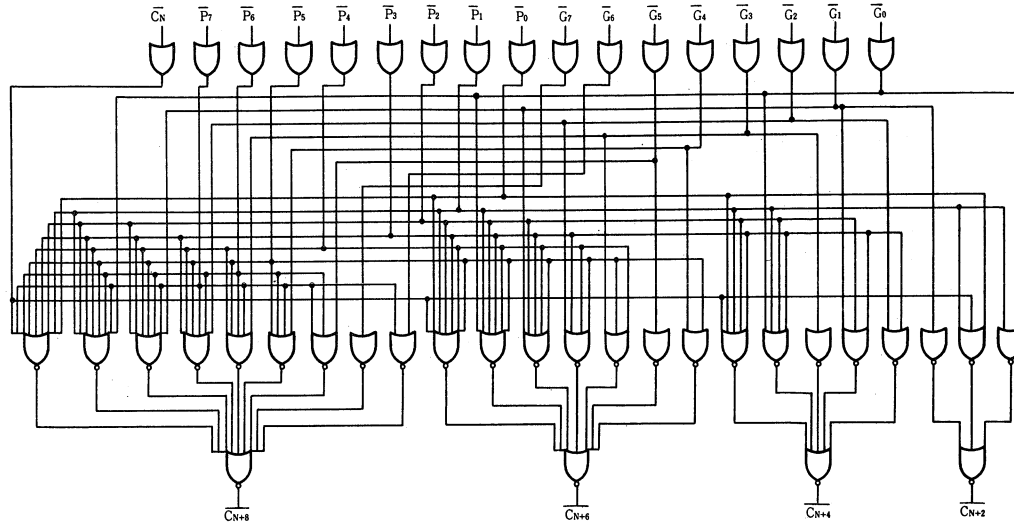
$\overline{C_{N+6}} = \overline{G_5} \cdot (\overline{P_5} + \overline{G_4}) \cdot (\overline{P_5} + \overline{P_4} + \overline{G_3}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{G_2}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{G_1}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{P_0} + \overline{C_N})$

● $\overline{C_{N+8}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	$\overline{G_4}$	$\overline{P_4}$	$\overline{G_5}$	$\overline{P_5}$	$\overline{G_6}$	$\overline{P_6}$	$\overline{G_7}$	$\overline{P_7}$	$\overline{C_{N+8}}$
×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	L	×	L
×	×	×	×	×	×	×	×	×	×	×	×	×	L	×	×	L	L
×	×	×	×	×	×	×	×	×	×	×	L	×	×	L	×	L	L
×	×	×	×	×	×	×	×	×	L	×	×	L	×	L	×	L	L
×	×	×	×	×	×	×	L	×	×	L	×	L	×	L	×	L	L
×	×	×	×	×	L	×	×	L	×	L	×	L	×	L	×	L	L
×	×	×	L	×	×	L	×	L	×	L	×	L	×	L	×	L	L
×	L	×	×	L	×	L	×	L	×	L	×	L	×	L	×	L	L
L	×	L	×	L	×	L	×	L	×	L	×	L	×	L	×	L	L
All other combinations																	H

$\overline{C_{N+8}} = \overline{G_7} \cdot (\overline{P_7} + \overline{G_6}) \cdot (\overline{P_7} + \overline{P_6} + \overline{G_5}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{G_4}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{G_3}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{G_2}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{G_1}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{P_0} + \overline{C_N})$

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		115	165	231	mA
Input Current	I_{IH}	$V_{IH}=V_{IH}$ max	$\overline{G_n}$ input	—	—	250	μA
			$\overline{P_n}$ input	—	—	340	
	I_{IL}	$V_{IH}=V_{IL}$ min		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ max or $V_{IN}=V_{IL}$ min	$R_T=50\Omega$, $V_{TT}=-2.0V$	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH}$ min or $V_{IN}=V_{IH}$ max	$R_T=50\Omega$, $V_{TT}=-2.0V$	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5V$, $V_{CC}=2.0V$, $Ta=25°C$)

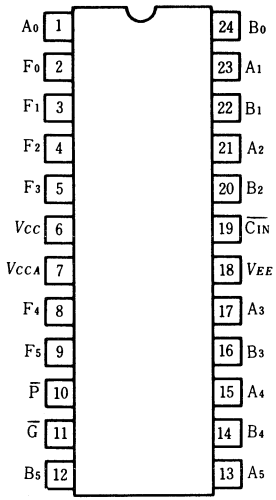
Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	1.10	1.80	2.60	ns
Transition Time	t_{TLH}, t_{THL}		0.40	1.00	1.60	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Fast 6-bit Adders

The HD100180 is a High Speed 6-bit Adder capables of performing as full 6-bit addition of 2 operands in 2ns.
Inputs for the adder are active low Carry-In, Operand A, and Operand B; outputs are Function, active low Carry Generate, and active low Carry Propagate. When used with the HD100179, Full Carry Lookahead, as a second order Lookahead Block. HD100180 provides high speed addition of very long words.

■PIN ARRANGEMENT

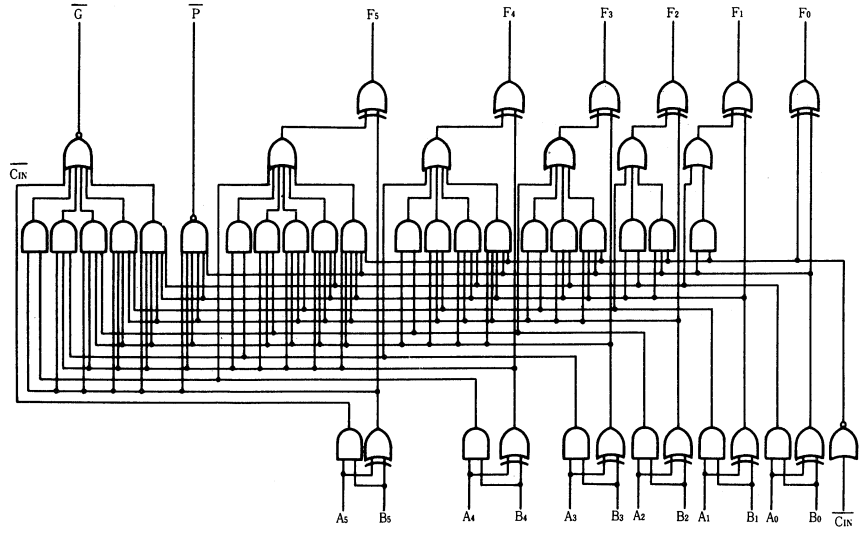


(Top View)

■LOGIC FUNCTION

$F_0 = P_0 \oplus C_{IN}$
$F_1 = P_1 \oplus (G_0 + P_0 C_{IN})$
$F_2 = P_2 \oplus (G_1 + P_1 G_0 + P_1 P_0 C_{IN})$
$F_3 = P_3 \oplus (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{IN})$
$F_4 = P_4 \oplus (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 G_0 C_{IN})$
$F_5 = P_5 \oplus (G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 G_0 + P_4 P_3 P_2 P_1 P_0 C_{IN})$
$\overline{P} = \overline{P_0 P_1 P_2 P_3 P_4 P_5}$
$\overline{G} = \overline{G_5 + P_5 G_4 + P_5 P_4 G_3 + P_5 P_4 P_3 G_2 + P_5 P_4 P_3 P_2 G_1 + P_5 P_4 P_3 P_2 P_1 G_0}$
$P_0 = A_0 \oplus B_0$
$P_1 = A_1 \oplus B_1$
$P_2 = A_2 \oplus B_2$
$P_3 = A_3 \oplus B_3$
$P_4 = A_4 \oplus B_4$
$P_5 = A_5 \oplus B_5$

■LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE}=−4.5V, V_{CC}=GND, Ta=0～+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		137	195	255	mA
Input Current	I_{IH}	$V_{IN}=V_{IH}$ max		—	—	220	μA
	I_{IL}	$V_{IN}=V_{IL}$ min		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ max or $V_{IN}=V_{IL}$ min	R_T=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH}$ min or $V_{IN}=V_{IL}$ max	R_T=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE}=−2.5V, V_{CC}=2.0V, Ta=25°C)

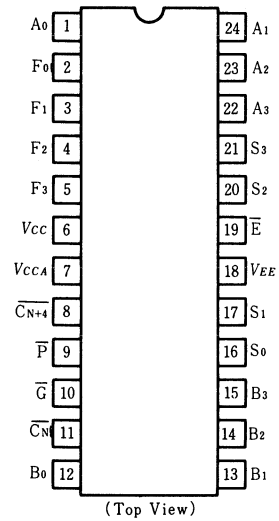
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	An/Bn→Fn	1.20	2.25	3.55	ns
			An/Bn→Pn	1.00	1.90	2.95	
			An/Bn→Gn	1.30	2.10	3.20	
			$\overline{C_{IN}}$ → Fn	1.00	2.10	3.45	
Transition Time	t_{TLH}, t_{THL}			0.50	1.30	2.40	ns

4-bit Binary/BCD ALU

The HD100181 performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (Sn) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable ($\overline{E}$) input open makes the latches transparent.

The circuit uses internal lookahead carry to minimize delay to the F outputs and to the ripple Carry Output, $\overline{Cn+4}$. Group carry lookahead Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are also provided, which are independent of the carry In $\overline{Co}$. The $\overline{P}$ output goes low when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, $\overline{G}$ goes low when the sum of A and B is greater than fifteen (nine for BCD) in plus mode, or when their difference is greater than zero in a minus mode.

■PIN ARRANGEMENT

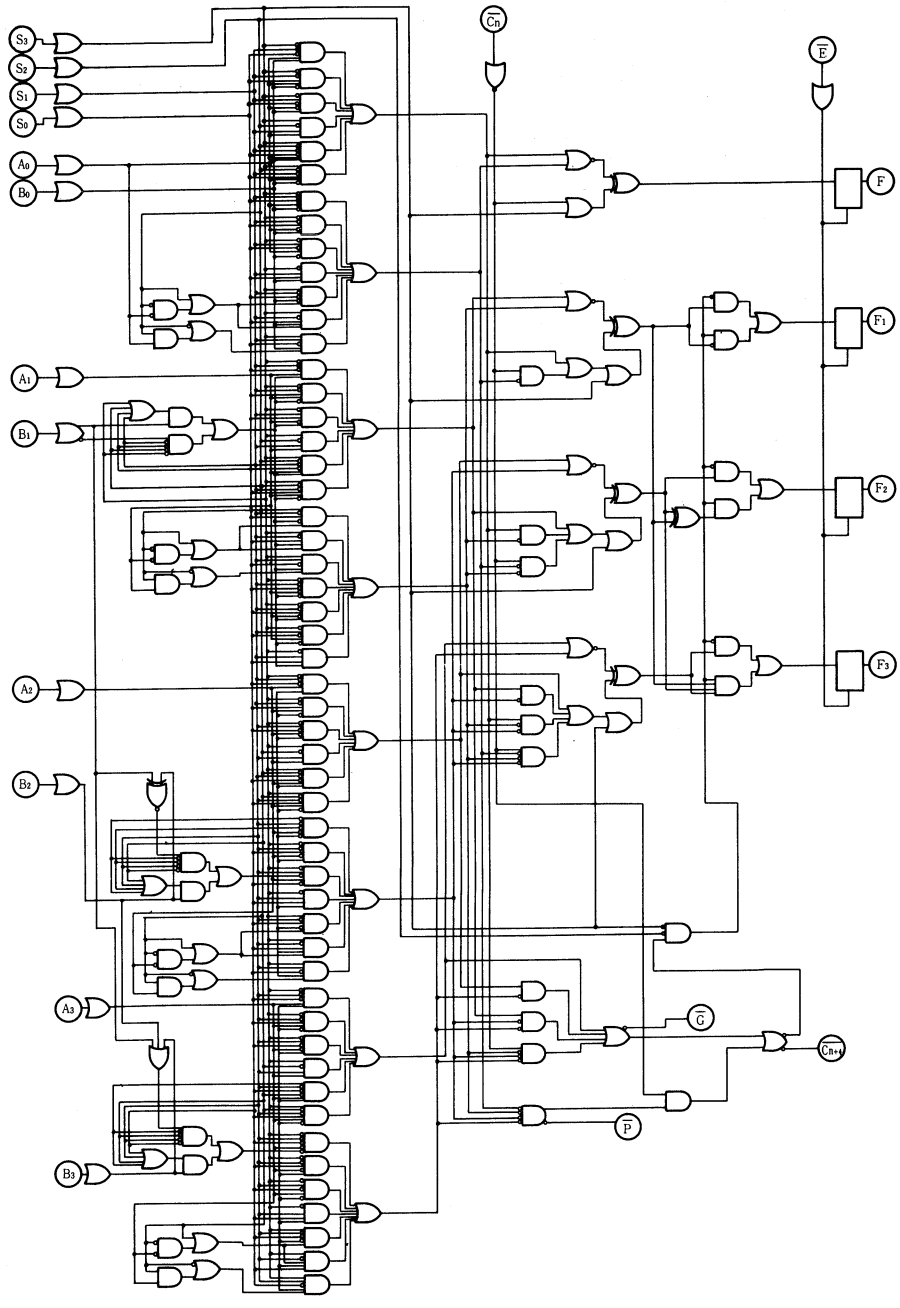


(Top View)

■FUNCTION SELECT TABLE

S_3	S_2	S_1	S_0	Function
L	L	L	L	A plus B BCD
L	L	L	H	A minus B BCD
L	L	H	L	B minus A BCD
L	L	H	H	0 minus B BCD
L	H	L	L	A plus B Binary
L	H	L	H	A minus B Binary
L	H	H	L	B minus A Binary
L	H	H	H	0 minus B Binary
H	L	L	L	$Fn=AnBn+\overline{An}\overline{Bn}$
H	L	L	H	$Fn=An\overline{Bn}+\overline{An}Bn$
H	L	H	L	$Fn=An+Bn$
H	L	H	H	$Fn=An$
H	H	L	L	$Fn=\overline{Bn}$
H	H	L	H	$Fn=Bn$
H	H	H	L	$Fn=AnBn$
H	H	H	H	Fn=Low

■LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		135	195	270	mA
Input Current	I_{IH}	$V_{IN}=V_{IH}$ max	Sn, $\overline{E}$ input	—	—	350	μA
			Other inputs	—	—	250	μA
	I_{IL}	$V_{IN}=V_{IL}$ min		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ max or $V_{IN}=V_{IL}$ min	R_T=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH}$ min or $V_{IN}=V_{IL}$ max	R_T=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveforms	$\overline{Co}$→Fn	1.60	3.00	4.60	ns
			$\overline{Co}$→$\overline{Cn+4}$	1.50	2.45	3.60	
			An, Bn→$\overline{P}$, $\overline{G}$	1.40	2.80	4.40	
			Sn→$\overline{P}$, $\overline{G}$	2.00	3.50	5.10	
			An, Bn→$\overline{Cn+4}$	2.00	3.85	5.70	
			Sn→$\overline{Cn+4}$	2.80	4.80	6.75	
			An, Bn→Fn	2.10	4.00	6.20	
			Sn→Fn	1.50	4.30	7.10	
			$\overline{E}$→Fn	1.30	2.00	3.00	
Transition Time	t_{TLH}, t_{THL}			0.50	1.00	3.50	ns
Set-up Time	t_{su}		An, Bn→$\overline{E}$	4.05	—	—	ns
			Sn→$\overline{E}$	5.15	—	—	
			$\overline{Cn}$→$\overline{E}$	2.35	—	—	
Hold Time	t_h		An, Bn→$\overline{E}$	0.20	—	—	ns
			Sn→$\overline{E}$	0.95	—	—	
			$\overline{Cn}$→$\overline{E}$	0.80	—	—	

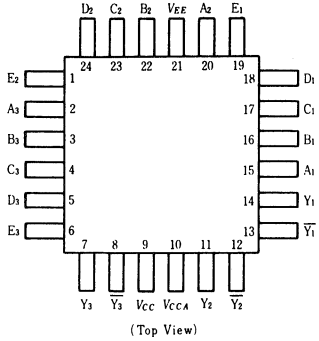
Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100KF Series

HD100101F

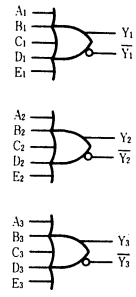
Triple 5-input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		18	26	38	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$		—	—	350	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}		$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$°C)

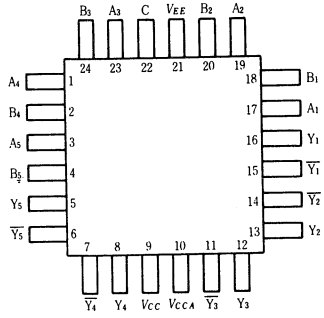
Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveforms	0.45	0.75	0.95	ns
	t_{PHL}					
Transition Time	t_{TLH}		0.45	0.70	1.10	ns
	t_{THL}					

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100102F

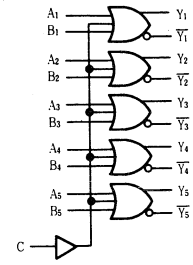
Quintuple 2-input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			38	55	80	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	Pin 22		—	—	300	μA
			All input except pin 22		—	—	350	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}			$V_{TT}=-2.0V$	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}			$V_{TT}=-2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5V$, $V_{CC}=2.0V$, $Ta=25°C$)

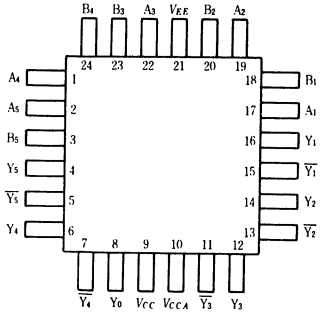
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveforms	All input except pin 22	0.45	0.75	0.95	ns
	t_{PHL}		Pin 22	0.90	1.50	1.95	ns
Transition Time	t_{TLH}			0.50	0.70	1.10	ns
	t_{THL}						

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100107F

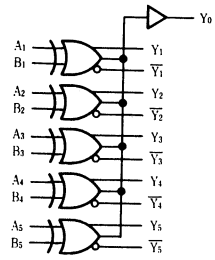
Quintuple Exclusive-OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			46	66	96	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	Pin 3, 18, 20, 23, 24		—	—	250	μA
			Pin 1, 2, 17, 19, 22		—	—	350	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}			$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}			$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$°C)

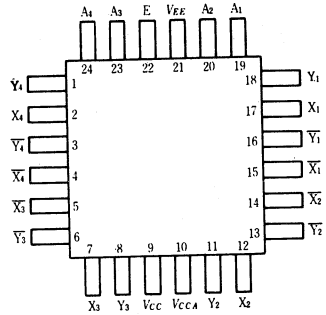
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveforms	Pin 3, 18, 20, 23, 24	0.55	1.10	1.55	ns
			Pin 1, 2, 17, 19, 22	0.55	0.90	1.20	ns
			Pin 8	1.15	1.85	2.55	ns
Transition Time	t_{TLH} t_{THL}			0.45	0.70	1.20	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100112F

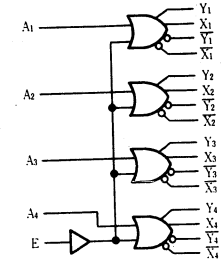
Quadruple Drivers

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$℃)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			51	73	106	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	Pin 22		—	—	450	μA
			All input except pin 22		—	—	550	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}			$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}			$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	Enable(Common input)	0.85	1.30	1.70	ns
	t_{PHL}		Data	0.55	0.90	1.20	ns
Transition Time	t_{TLH}			0.45	0.90	1.40	ns
	t_{THL}						

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

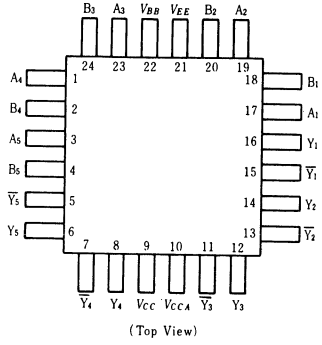
HD100114F

Quintuple Differential Line Receivers

The HD100114F is a Quint. Differential Amp. with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single ended reception. Active current sources provide common mode rejection of 1.5V in either the positive or negative direction.

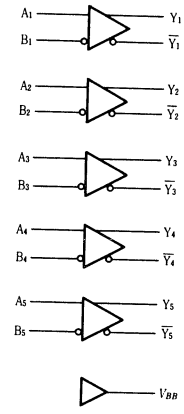
A defined output state exists if both inputs are at the same potential between and including $-V_{EE}$ and V_{CC}. The defined state is logic high on outputs $\overline{Yn}$.

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■TRUTH TABLE

Input		Output	
A_n	B_n	Y_n	$\overline{Y_n}$
H	V_{BB}	H	L
L	V_{BB}	L	H
V_{BB}	H	L	H
V_{BB}	L	H	L
$A_n - B_n \geqq 0.15$ V		H	L
$A_n - B_n \leqq 0.0$ V		L	H
$0.0 < A_n - B_n < 0.15$ V		*	*
Open	Open	L	H
V_{CC}	V_{CC}	L	H
V_{EE}	V_{EE}	L	H

H = High level
L = Low level
V_{BB} = Base bias voltage
* = Undefined

■DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	$A_n = V_{BB}$, $B_n = V_{IL\ min}$	51	73	106	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$, $A_n = V_{BB}$, $B_n = V_{IL\ min}$	—	20	50	μA
Leakage Current	I_{CBO}	$V_{IN} = V_{EE}$, $A_n = V_{BB}$, $B_n = V_{IL\ min}$	—	—	1.0	μA
Common Mode Voltage	V_{CM}	Permissible V_{CM} with respect to V_{BB}	−2.30	—	−0.55	V
Reference Voltage	V_{BB}	Tie pins 1, 3, 17, 19, 23 to pin 22	−1380	−1320	−1260	mV
Input Voltage Differential	V_{DIFF}		—	150	—	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

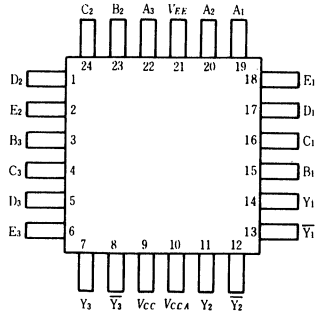
Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	0.65	1.20	1.80	ns
Transition Time	t_{THL} t_{TLH}		0.45	0.90	1.30	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100117F

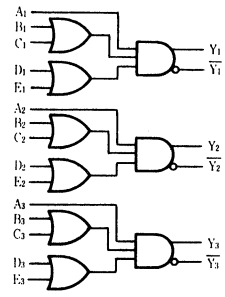
Triple 2-wide OR-AND/OR-AND-INVERT Gates

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		37	54	79	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	Pin 19, 20, 22	—	—	350	μA
			All input except pin 19, 20, 22	—	—	220	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}		$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$°C)

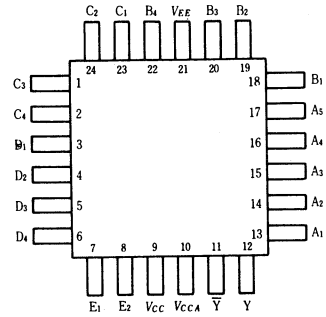
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	All input except pin 19, 20, 22	0.95	1.55	2.10	ns
	t_{PHL}		Pin 19, 20, 22	0.45	0.75	0.95	ns
Transition Time	t_{TLH}			0.45	0.75	1.10	ns
	t_{THL}						

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100118F

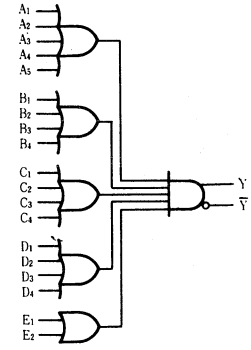
5-wide OR-AND/OR-AND-INVERT Gates

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			27	39	57	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	A input		—	—	350	μA
			B~E input		—	—	240	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		$R_T=50\Omega$	−1025	−955	−880	mV
	V_{OL}			$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_T=50\Omega$	−1035	—	—	mV
	V_{OLC}			$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	0.85	1.40	1.90	ns
	t_{PHL}					
Transition Time	t_{TLH}		0.35	0.75	1.20	ns
	t_{THL}					

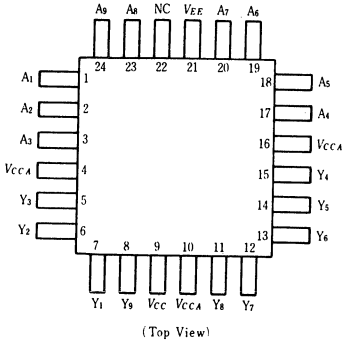
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100122F

9-bit Buffers

The HD100122F contains nine independent, high speed, buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus oriented systems where minimal output loading or bus isolation is desired.

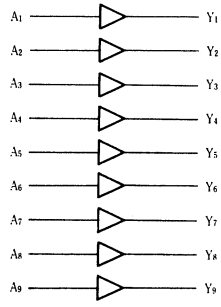
■PIN ARRANGEMENT



(Top View)

Note) NC : No connection

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		47	70	95.5	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$		—	—	350	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_T=50\Omega$	−1025	−955	−880	mV
	V_{OL}		$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_T=50\Omega$	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	0.45	0.90	1.25	ns
	t_{PHL}					
Transition Time	t_{TLH}		0.45	0.90	1.30	ns
	t_{THL}					

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100123F

Hex Bus Drivers

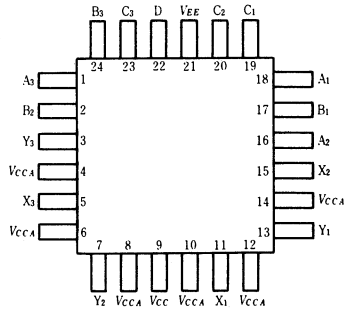
The HD100123F contains six bus drivers capable of driving terminated lines with terminations as low as 25Ω. To reduce crosstalk, each output has its respective ground connection and transition times were designed to be longer than on other HD100K devices.

The driver itself performs the positive logic AND of a data input (A, B inputs) and the OR of two select inputs (C, D inputs).

The output voltage low level is designed to be more negative than normal ECL outputs.

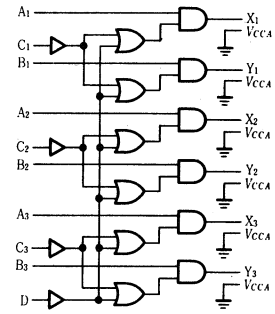
This allows an emitter-follower output transistor to turn off when the termination supply is −2.0V ±10%, and thus present a high impedance to the data bus.

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			113	162	235	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	A, B, C input		—	—	230	μA
			D input		—	—	330	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or	R_T = 25Ω	V_{TT} = −2.0 V	−1025	−955	−880	mV
	V_{OL}	$V_{IN} = V_{IL\ min}$		V_{TT} = −2.3 V	—	—	−2200	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or	R_T = 25Ω	V_{TT} = −2.0 V	−1035	—	—	mV
	V_{OLC}	$V_{IN} = V_{IL\ max}$		V_{TT} = −2.3 V	—	—	−2200	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

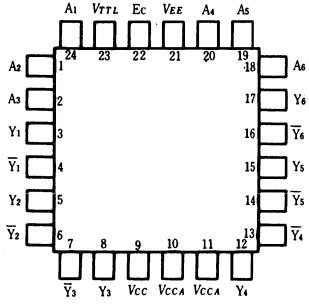
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	A, B input	1.95	3.00	4.00	ns
	t_{PHL}			1.00	1.45	1.90	
	t_{PLH}		C input	2.15	3.40	4.30	
	t_{PHL}			1.20	1.80	2.38	
	t_{PLH}		D input	2.30	3.50	4.70	
	t_{PHL}			1.20	1.80	2.35	
Transition Time	t_{TLH}			0.80	1.30	1.90	ns
	t_{THL}			0.45	0.80	1.20	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Hex TTL-to-ECL Translators

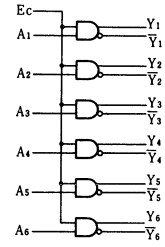
The HD100124F is a Hex Translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or with Schottky TTL. A Common Enable input (E_C), when low, holds all inverting outputs high and holds all True outputs low.
The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensate. When the circuit is used in the differential mode, the HD100124F, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $V_{TTL}=5V$, $Ta=0\sim+85°C$)

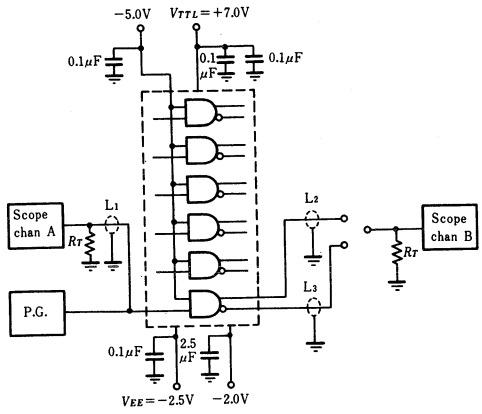
Item		Symbol	Test Condition	min	typ	max	Unit
Input Voltage		V_{IH}	Guaranteed Input Voltage High for All Inputs	2.0	—	5.0	V
		V_{IL}	Guaranteed Input Voltage Low for All Inputs	0	—	0.8	V
Clamp Input Voltage		V_{CD}	$I_{IN}=-10mA$	−1.5	—	—	V
Input Breakdown Voltage		V_{BO}	$I_{IN}=1.0mA$, Other Inputs $V_{IN}=GND$	5.5	—	—	V
Input Current	A inputs	I_{IH}	$V_{IN}=2.4V$, Ec $V_{IN}=0.4V$	—	—	50	μA
		I_{IL}	$V_{IN}=0.4V$, Ec $V_{IN}=4.0V$	−3.2	—	—	mA
	Ec input	I_{IHX}	Ec $V_{IN}=2.4V$, All Other Inputs $V_{IN}=0.4V$	—	—	300	μA
		I_{ILX}	Ec $V_{IN}=0.4V$, All Other Inputs $V_{IN}=4.0V$	−16.0	—	—	mA
Power Supply Current		I_{EE}	Inputs and Outputs Open	52	85	106	mA
		I_{CCH}	All Inputs $V_{IN}=4.0V$	—	41	56	mA
		I_{CCL}	All Inputs $V_{IN}=GND$	—	41	61	mA

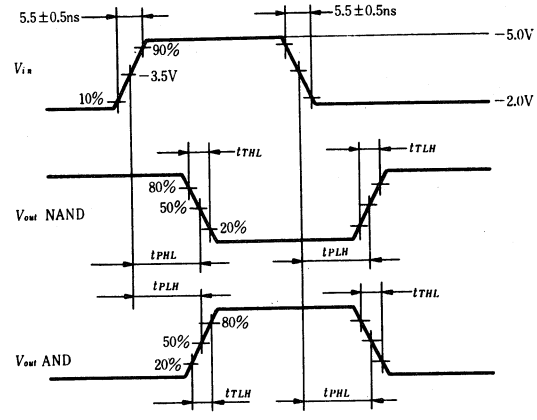
■AC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $V_{TTL}=5.0V$, $Ta=25°C$)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See Test Circuit and Waveform	0.50	1.60	2.70	ns
Transition Time	t_{TLH}, t_{THL}		0.60	1.20	2.20	ns

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

■ SWITCHING TIME TEST CIRCUIT AND WAVEFORM



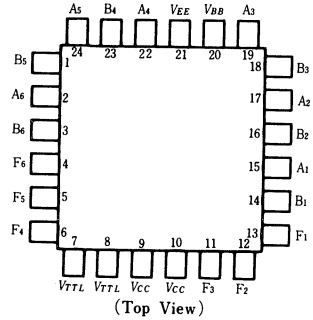


Notes) 1. L_1, L_2 and L_3 are equal lengths of 50Ω impedance lines.
2. R_T equals 50Ω termination of scope.

Hex ECL-to-TTL Translators

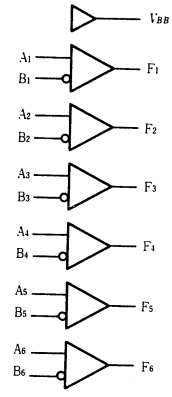
The HD100125F is a Hex Translator for converting HD100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or as a differential receiver. An internal reference voltage generator provides V_{BB} on pin 17 for single-ended operation or for use in Schmitt trigger applications. The outputs, which will go low when the inputs are left unconnected, have a fan-out of 10 Schottky TTL loads. When used in the differential mode, the inputs have a common mode rejection of −1V, making this device tolerant of ground offsets and transients between the signal source and the translator.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Inputs		Output
In	$\overline{In}$	On
L	H	L
H	L	H
L	L	*
H	H	*
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

* Undetermind.

■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND = 0V, V_{TTL} = 5.0V, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	$I_{OH}=-2.0$mA	2.5	—	—	V
	V_{OL}		$I_{OL}=20$mA	—	—	0.5	V
	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	$I_{OH}=-2.0$mA	2.5	—	—	V
	V_{OLC}		$I_{OL}=20$mA	—	—	0.5	V
Common Mode Voltage	V_{CM}	V_{CM} ref. to V_{BB} (Notes 1)		—	—	1.0	V
Input Voltage Differential	V_{DIFF}	Required for full output voltage swing		150	—	—	mV
Reference Voltage	V_{BB}	$V_{IN}=V_{ILB}$		−1380	−1320	−1260	mV
Input Current	I_{IL}	$V_{IN}=V_{EE}$ (Notes 2)		−0.5	—	—	μA
	I_{IH}	$V_{IN}=V_{IHA}$ (Notes 2)		—	—	350	μA
Short Circuit Current	I_{OS}	V_{IN}=GND (Notes 3)		−100	—	−40	mA
Power Supply Current	I_{EE}	Inputs and Outputs Open		36	65	85	mA
TTL Drive Current	I_{TTL}	$V_{IN}=V_{ILB}$ (Notes 4)		50	88	115	mA

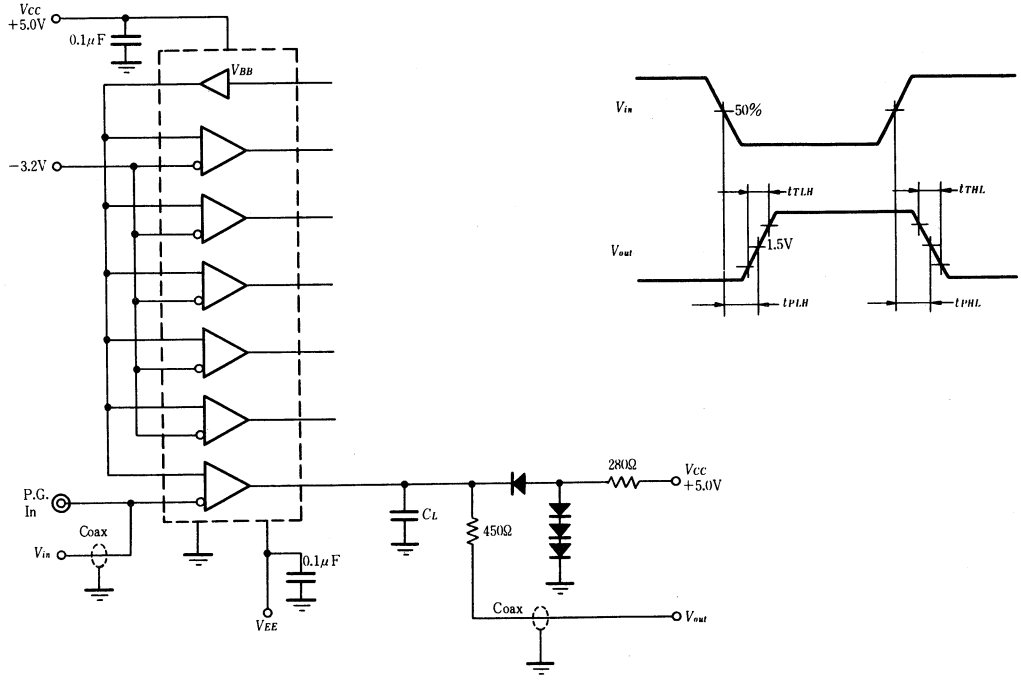
Notes) 1. $V_{CM}=V_{BB}\pm1$V (V_{DIFF} = 150 mV)
2. Complementary Input = V_{BB}
3. One Output at a Time
4. True Inputs = V_{BB}, Complementary Inputs = V_{ILB}

■ AC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = 0V, V_{TTL} = 5.0V, Ta = 25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See Test Circuit and Waveform	1.10	2.20	3.50	ns
Transition Time	t_{TLH}, t_{THL}		—	0.60	1.50	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5 m/s (500 linear fpm) is maintained.

■ SWITCHING TIME TEST CIRCUIT AND WAVEFORM



Notes) 1. 50Ω termination to ground located in each scope channel input.
2. All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be ½ inch from TPin to input pin and TPout to output pin.
3. C_L=25pF including.
4. One input from each gate must be tied to V_{BB}

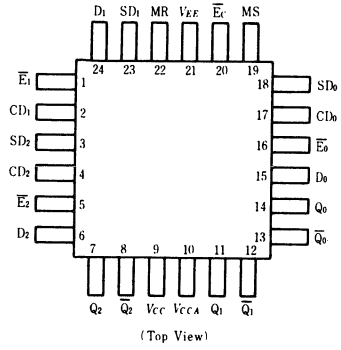
Triple D-type Latches

The HD100130F contains three D-type latches with true and complement outputs and with Common Enable ($\overline{Ec}$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{En}$), Direct Set (SDn) and Direct Clear (CDn) inputs.

The Q output follows its Data (D) input when both $\overline{En}$ and $\overline{Ec}$ are low. When either $\overline{En}$ or $\overline{Ec}$ or both are high, a latch stores the last valid data present on its Dn input before $\overline{En}$ or $\overline{Ec}$ went high. Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs.

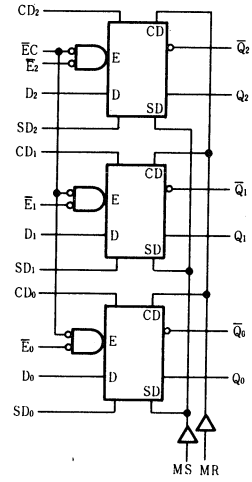
The individual CDn and SDn also override the Enable inputs.

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■TRUTH TABLE

D_n	$\overline{E_n}$	$\overline{Ec}$	MS SD_n	MR CD_n	Q_n
L	L	L	L	L	L
H	L	L	L	L	H
×	H	×	L	L	*
×	×	H	L	L	*
×	×	×	H	L	H
×	×	×	L	H	L
×	×	×	H	H	U

H = High level
L = Low level
× = Immaterial
* = Ratains data present before $\overline{E}$ positive transition
U = Undefined

■DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			61	88	128	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	D_n input		—	—	350	μA
			CD_n, SD_n input		—	—	530	
			$\overline{E}_n$ input		—	—	240	
			$\overline{E}_C$, MR, MS input		—	—	450	
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		R_T = 50Ω	−1025	−955	−880	mV
	V_{OL}			V_{TT} = −2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		R_T = 50Ω	−1035	—	—	mV
	V_{OLC}			V_{TT} = −2.0V	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	Fig. 1	D_n input	0.50	0.85	1.10	ns
			CD_n, SD_n, $\overline{E}_n$ input	0.65	1.10	1.45	
			$\overline{E}_C$ input	0.70	1.20	1.55	
			MS, MR input	1.10	1.85	2.20	
Transition Time	t_{TLH}, t_{THL}			0.40	0.90	1.30	ns
Set-up Time	t_{su}	Fig. 2	D_n input	0.60	—	—	ns
			CD_n, SD_n input (Release Time)	1.20	—	—	
			MR, MS input (Release Time)	2.00	—	—	
Hold Time	t_h		D_n input	0.00	—	—	ns
Pulse Width	t_{PW}		$\overline{E}_n$, $\overline{E}_C$ (Low)	1.00	—	—	ns
			CD_n, SD_n, MR, MS (High)	1.15	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

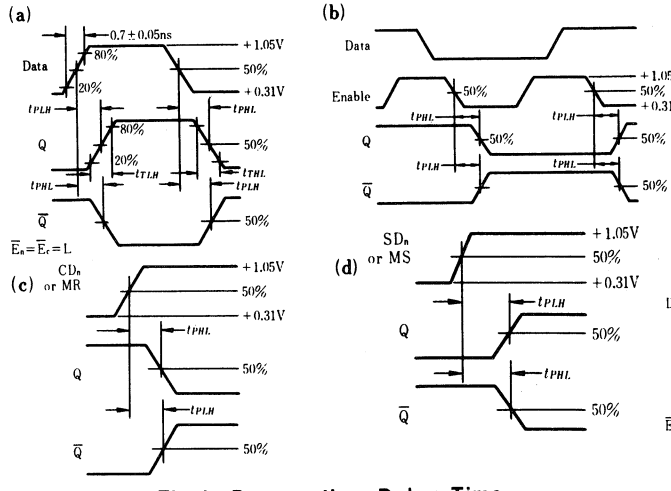


Fig.1 Propagation Delay Time

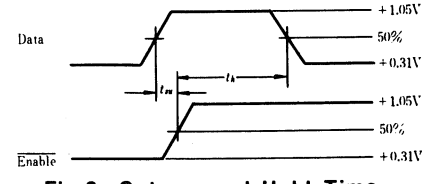


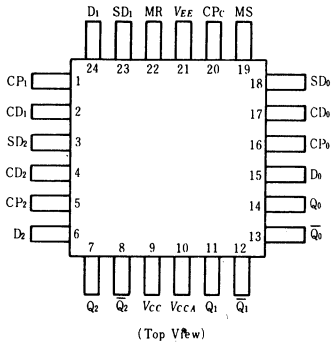
Fig.2 Set-up, and Hold Time

HD100131F

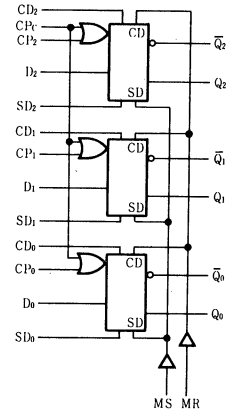
Triple D-type Flip-Flops

The HD100131F contains three D-type Master-Slave Flip-Flops with true and complement outputs, a Common Clock (CPc), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual clocks (CPn), Direct Set (SDn) and Direct Clear (CDn) inputs. Data enters a master when both CPn and CPc are low and transfers to a slave when CPn or CPc (or both) go high.
The Master Set, Master Reset and individual CDn and SDn inputs override the Clock inputs.

■PIN ARRANGEMENT



■LOGIC DIAGRAM



■TRUTH TABLE

D_n	CP_n	CP_C	MS SD_n	MR CD_n	Q_{n+1}
L	↑	L	L	L	L
H	↑	L	L	L	H
L	L	↑	L	L	L
H	L	↑	L	L	H
×	H	×	L	L	Q_n
×	×	H	L	L	Q_n
×	×	×	H	L	H
×	×	×	L	H	L
×	×	×	H	H	U

H = High level
L = Low level
× = Immaterial
U = Undefined
↑ = Clock transition from low level to high level

■DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			74	106	149	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	CP_n, D_n input		—	—	240	μA
			MS, MR, CP_C input		—	—	450	
			CD_n, SD_n input		—	—	530	
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		$R_T=50\Omega$ $V_{TT}=-2.0V$	−1025	−955	−880	mV
	V_{OL}				−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_T=50\Omega$ $V_{TT}=-2.0V$	−1035	—	—	mV
	V_{OLC}				—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5V$, $V_{CC}=2.0V$, $Ta=25°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	Fig. 1	CP_C input	0.75	1.25	1.65	ns
			CDn, SDn input (CP=H)	1.00	1.55	2.00	
			CDn, SDn input (CP=L)	0.60	1.15	1.50	
			CPn input	0.70	1.15	1.50	
			MS, MR input (CP=H)	1.05	1.90	2.75	
			MS, MP input (CP=L)	0.95	1.70	2.45	
Transition Time	t_{TLH} t_{THL}			0.35	0.90	1.30	ns
Set-up Time	t_{su}	Fig. 2	Dn input	0.60	—	—	ns
			CDn, SDn input (Release Time)	1.20	—	—	
			MS, MR input (Release Time)	2.00	—	—	
Hold Time	t_h		Dn input	−0.20	—	—	ns
Toggle Frequency	f_{tog}	Fig. 3		300	—	—	MHz
Pulse Width	t_{PW}		CPn, CPc (Low)	0.75	—	—	ns
			CDn, SDn, MR, MS (High)	1.15	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

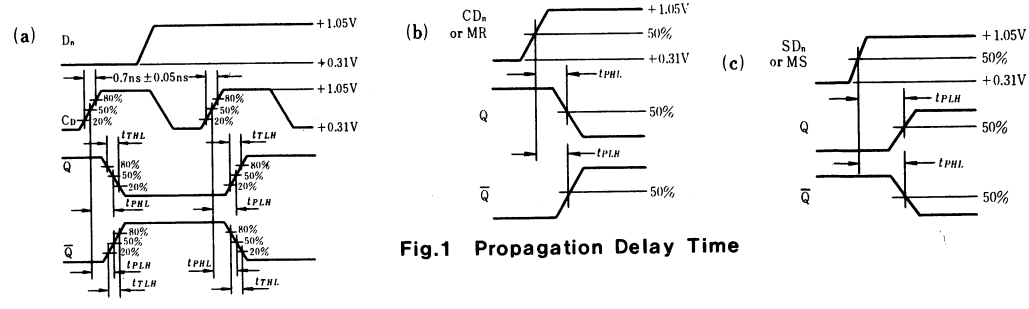


Fig.1 Propagation Delay Time

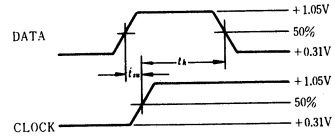


Fig.2 Set-up, and Hold Time

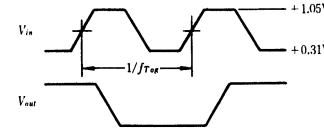


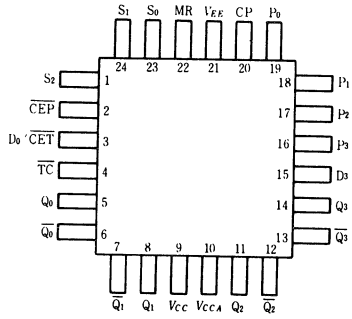
Fig.3 Toggle Frequency

4-stage Counter/Shift Register

The HD100136F operates a either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (Sn) inputs determine the mode of operation, as shown in the mode select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multi-stage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (Do) input for shift-up operation.

For shift-down operation D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes low when the counter reaches 15 in the count/up mode or 0 in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the Do/$\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multi-stage counting or shift-up operation. The individual Preset (Pn) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A high signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, asynchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops.

■PIN ARRANGEMENT



(Top View)

■FUNCTION SELECT TABLE

S_0	S_1	S_2	Function
L	L	L	Load
L	H	L	Shift down
H	H	L	Shift up
L	L	H	Count down
L	H	H	Count up
H	H	H	Hold
H	L	L	Complement
H	L	H	Clear

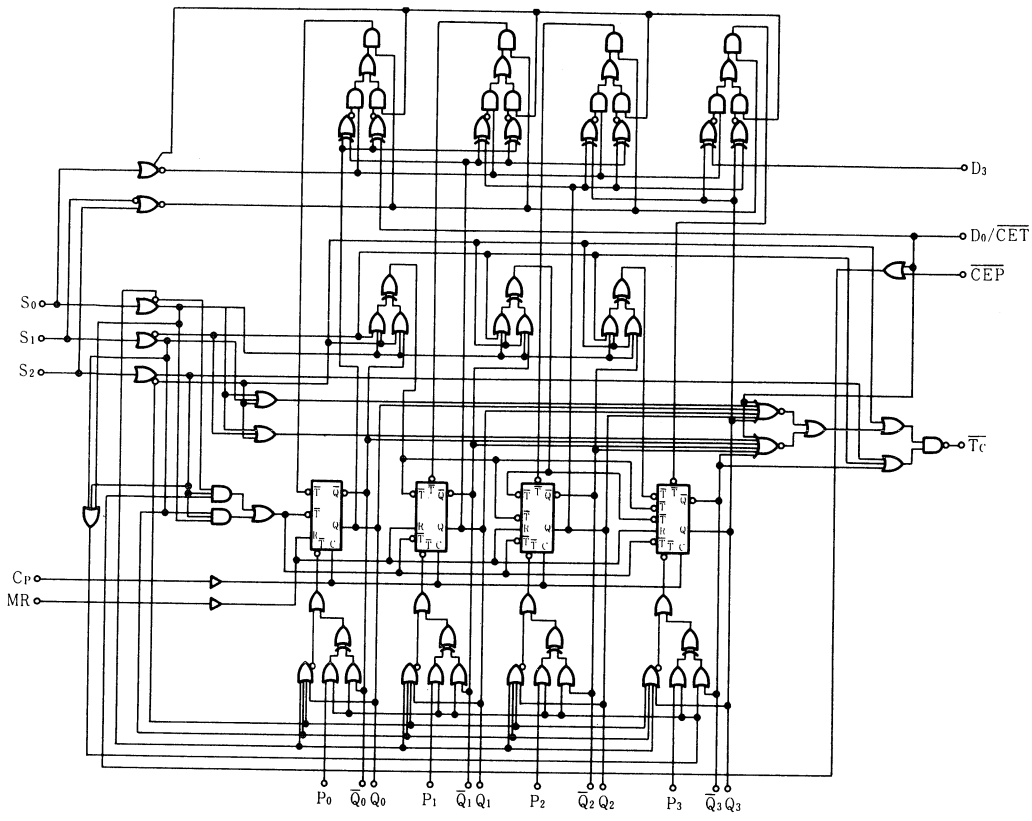
H = High level
L = Low level

■TRUTH TABLE

IN												OUT					Mode
S_0	S_1	S_2	CP	MR	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	P_3	P_2	P_1	P_0	Q_3	Q_2	Q_1	Q_0	TC	
L	L	L	↑	L	×	×	×	H	L	H	H	H	L	H	H	L	Load*
H	H	H	↑	L	×	×	×	×	×	×	×	H	L	H	H	H	Hold
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	L	L	H	
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	L	H	H	
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	H	L	H	Count up
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	H	H	L	(max)
L	H	H	↑	L	L	L	×	×	×	×	×	L	L	L	L	H	
L	H	H	↑	L	L	L	×	×	×	×	×	L	L	L	H	H	
L	H	H	×	L	L	H	×	×	×	×	×	L	L	L	H	H	($\overline{CET}$ inhibit)
L	H	H	×	L	H	L	×	×	×	×	×	L	L	L	H	H	($\overline{CEP}$ inhibit)
×	×	×	×	H	×	×	×	×	×	×	×	L	L	L	L	×	Clear (MR)
L	L	L	↑	L	×	×	×	L	H	L	L	L	H	L	L	L	Load*
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	H	H	H	
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	H	L	H	
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	L	H	H	Count down
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	L	L	L	(max)
L	L	H	↑	L	L	L	×	×	×	×	×	H	H	H	H	H	
L	L	H	↑	L	L	L	×	×	×	×	×	H	H	H	L	H	
H	L	L	↑	L	×	×	×	×	×	×	×	L	L	L	H	L	Complement
×	×	×	×	H	×	×	×	×	×	×	×	L	L	L	L	×	Clear (MR)
H	L	H	↑	L	×	×	×	×	×	×	×	L	L	L	L	H	Clear
H	H	L	↑	L	×	H	×	×	×	×	×	L	L	L	H	L	
H	H	L	↑	L	×	L	×	×	×	×	×	L	L	H	L	L	
H	H	L	↑	L	×	H	×	×	×	×	×	L	H	L	H	L	Shift up
H	H	L	↑	L	×	L	×	×	×	×	×	H	L	H	L	H	
×	×	×	×	H	×	×	×	×	×	×	×	L	L	L	L	×	Clear (MR)
L	H	L	↑	L	×	×	H	×	×	×	×	H	L	L	L	H	
L	H	L	↑	L	×	×	L	×	×	×	×	L	H	L	L	L	
L	H	L	↑	L	×	×	H	×	×	×	×	H	L	H	L	H	Shift down
L	H	L	↑	L	×	×	L	×	×	×	×	L	H	L	H	L	
×	×	×	×	H	×	×	×	×	×	×	×	L	L	L	L	×	Clear (MR)

× = Immaterial
* = each LOAD data
↑ = CP positive transition

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		136	195	283	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	Pn, Sn input	—	—	180	μA
			$\overline{CEP}$ input	—	—	200	
			MR input	—	—	240	
			D_3 input	—	—	280	
			CP input	—	—	390	
			$D_0/\overline{CET}$ input	—	—	530	
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_T=50\Omega$ $V_{TT}=-2.0$V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_T=50\Omega$ $V_{TT}=-2.0$V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	Fig. 1	CP to Q	0.95	1.64	2.15	ns
			CP to $\overline{TC}$	1.70	3.10	4.35	
			MR to Q	1.35	2.00	2.65	
			MR to $\overline{TC}$	1.80	3.50	5.35	
			Do/$\overline{CET}$ to $\overline{TC}$	1.40	2.60	3.65	
			Sn to $\overline{TC}$	1.20	2.25	3.25	
Transition Time	t_{TLH} t_{THL}			0.40	0.90	1.70	ns
Set-up Time	t_{su}	Fig. 2	Dn input	1.10	—	—	ns
			Pn input	1.55	—	—	
			Do/$\overline{CET}$, $\overline{CEP}$ input	1.50	—	—	
			Sn input	3.35	—	—	
			MR (Release Time)	2.50	—	—	
Hold Time	t_h		Dn input	−0.35	—	—	ns
			Pn input	−0.45	—	—	
			Do/$\overline{CET}$, $\overline{CEP}$ input	−0.05	—	—	
			Sn input	−0.85	—	—	
Toggle Frequency	f_{tog}	See test circuit and waveform		300	—	—	MHz
Pulse Width	t_{PW}		CP (High)	1.50	—	—	ns
			MR (High)	2.00	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

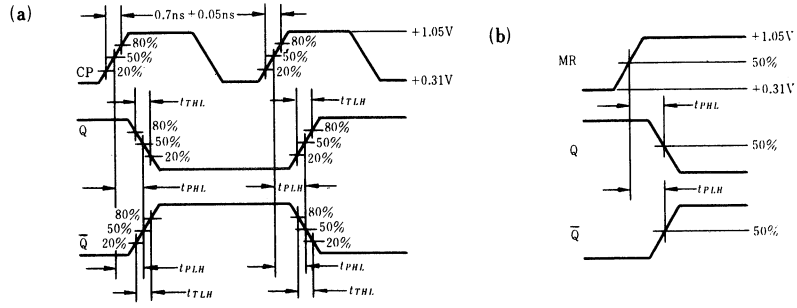


Fig.1 Propagation Delay Time

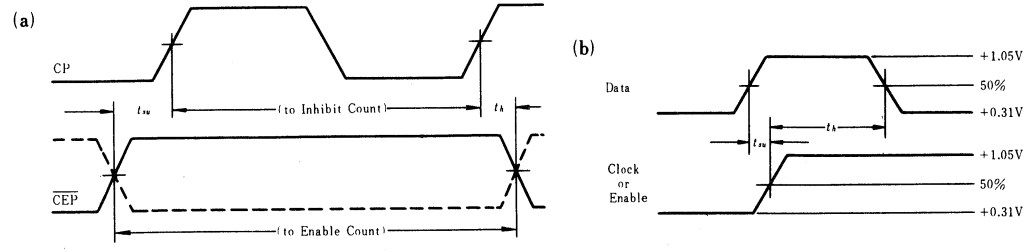


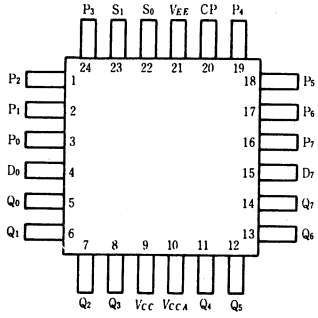
Fig.2 Set-up and Hold Time

8-bit Shift Registers

The HD100141F contains eight clocked D-type flip-flops with individual inputs (Pn) and outputs (Qn) for parallel operation, and with serial inputs (Dn) and steering logic for bidirectional shifting. The flip flops accept input data a set-up time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

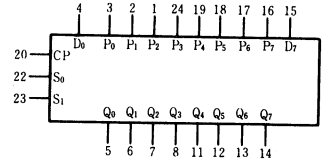
The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Function Sheet Table.

■PIN ARRANGEMENT



(Top View)

■LOGIC SYMBOL



■FUNCTION SHEET TABLE

Function	Input					Output							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↑	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↑	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↑	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	← No Change →							
Hold	X	X	X	X	H	← No Change →							
Hold	X	X	X	X	L	← No Change →							

H = High Level
L = Low Level
X = Don't Care
↑ = Low to High transition

■DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			119	170	238	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	CP input		—	—	640	μA
			Other input		—	—	220	
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		R_T=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}				−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		R_T=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}				—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PHL} t_{PLH}	Fig. 1		1.10	1.70	2.20	ns
Transition Time	t_{TLH} t_{THL}			0.40	—	0.95	ns
Shift Frequency	f_{shift}			380	500	—	MHz
Set-up Time	t_{su}	Fig. 2	Serial-in, Parallel-in	0.75	—	—	ns
			Select input	1.80	—	—	
Hold Time	t_h		Serial-in, Parallel-in	0.20	—	—	ns
			Select input	−0.80	—	—	
Pulse Width	t_{pw}		CP	0.75	—	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

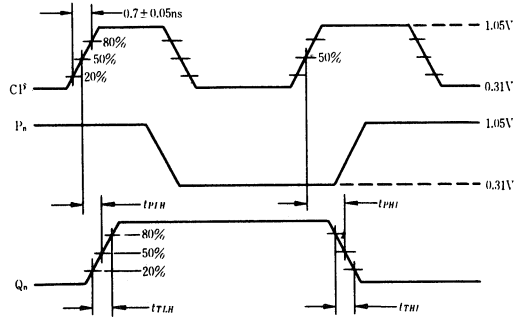


Fig.1 Propagation Delay Time

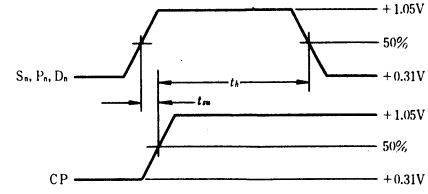


Fig.2 Set-up and Hold Time

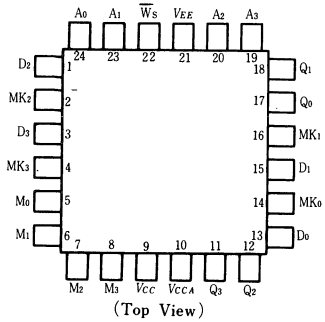
4×4 Content Addressable Memory

The HD100142F is a 4 word x 4 bit Content Addressable Memory (CAM). Each Word location has its own Address Select line. Reading or Writing is accomplished when the Address Select line is low. In the Read mode, Data from the addressed location appears at the Data (Qi) outputs.

A low Write Strobe selects the Write mode, a high Write Strobe select the Read mode. Each Data input has its own Mask input that blocks data storage when the Mask is high. The Data input word is simultaneously compared with each of the four memory Words.

If a Search Compare result in a Match, this output will go low. A high Mask input on any bit forces a Match of that bit. Each input has a 50kΩ (typical) pull-down resistor tied to V_{EE}. The outputs require external resistance terminations as they are not terminated internally through resistance to the V_{EE} supply.

■ PIN ARRANGEMENT



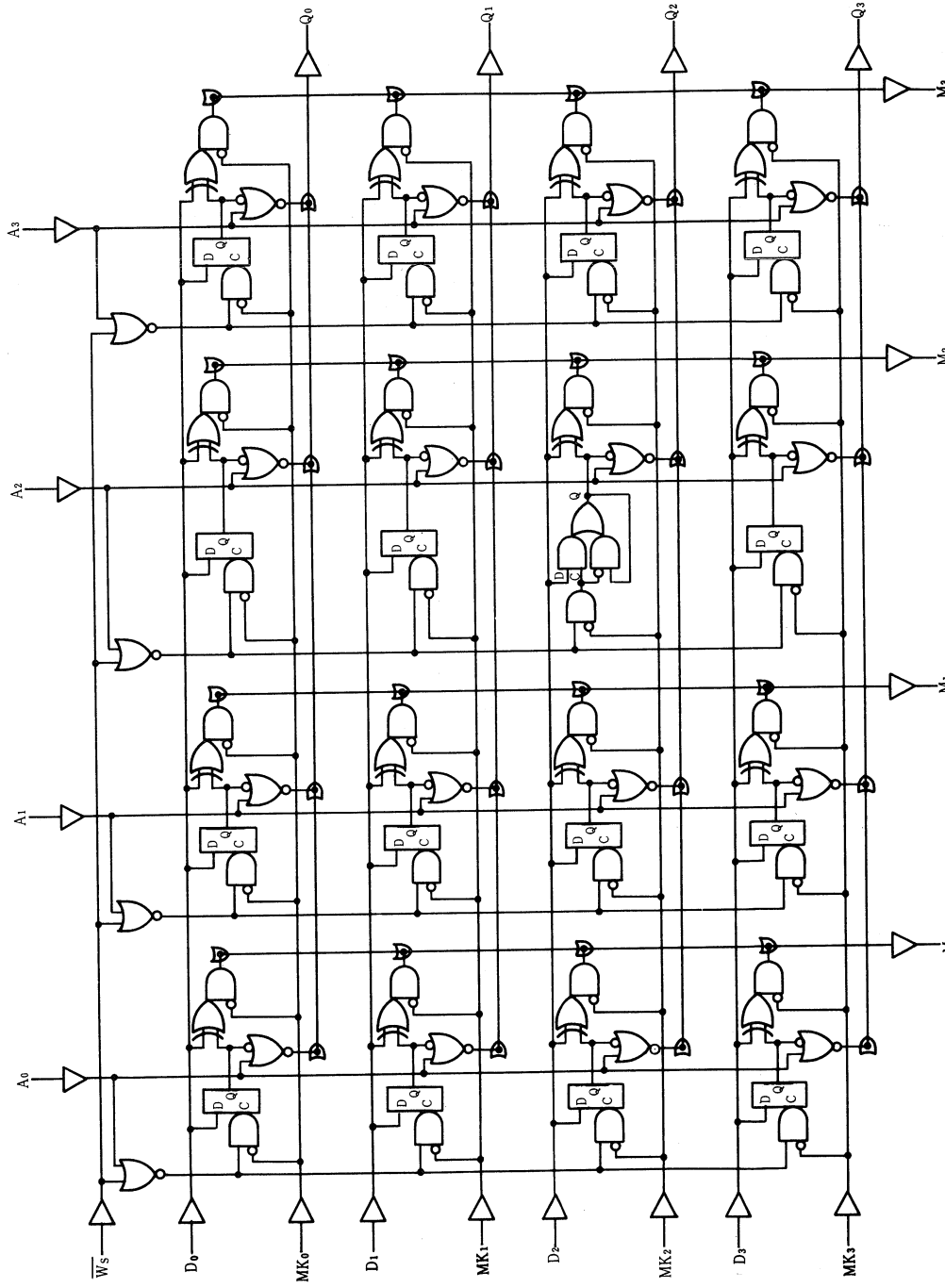
(Top View)

■ TRUTH TABLE

Operation	Inputs				Flip-Flop	Outputs	
	$\overline{W_S}$	A_i	D_j	MK_j	Q_{ij}	M_i	Q_j
	$\overline{W_S}$	A_0	D_0	MK_0		M_0	Q_0
		A_1	D_1	MK_1		M_1	Q_1
		A_2	D_2	MK_2		M_2	Q_2
		A_3	D_3	MK_3		M_3	Q_3
Write Disabled	×	H	×	×	NC	×	L
	×	L	×	H	NC	L	Q_{ijn-1}
	H	L	×	×	NC	×	Q_{ijn-1}
Write	L	L	H	L	H	L	H
	L	L	L	L	L	L	L
Read	H	L	×	×	H	×	H
	H	L	×	×	L	×	L
Match Masked	H	×	×	H	NC	L	×
Match Not Satisfied	H	L	H	L	L	H	L
	H	H	H	L	L	H	L
	H	H	L	L	H	H	L
	H	L	L	L	H	H	H
Match Satisfied	H	L	H	L	H	L	H
	H	H	H	L	H	L	L
	H	H	L	L	L	L	L
	H	L	L	L	L	L	L

H = High Voltage Level (Most Positive)
L = Low Voltage Level (Most Negative)
X = Don't Care (Maybe either high or low)
NC = No Change from Previous State
$\overline{W_S}$ = Write Strobe
A_i = Address for ith Word
D_j = Data for jth Bit
MK_j = Data mask for jth Bit (H = Mask)
Q_{ij} = Cell State for ith Word, jth Bit
M_i = Match Output of ith Word (L = True)
Q_j = Data Output of jth Bit
Q_{n+1} = Previous Cell State

■ LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		114	163	288	mA
Input Current	I_{IH}	$V_{IN}=V_{IL}$ max	$\overline{Ws}$, A_j input	—	—	159	μA
			D_n input	—	—	149	
			MK_n input	—	—	164	
	I_{IL}	$V_{IN}=V_{IL}$ min		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ max or $V_{IN}=V_{IL}$ min	R_T=50 Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH}$ min or $V_{IN}=V_{IL}$ max	R_T=50 Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Address to Data Out	t_{AD}	Fig. 2, 3	1.30	1.90	2.70	ns
Data In to Match Out Time	t_{DM}	Fig. 4	1.35	2.45	3.35	
Mask In to "Enable Partial" Match Out Time	t_{MM}		1.25	1.95	2.65	
Data In to New Data Out	t_{DD}	Fig. 2	1.90	3.00	4.25	
Write to New Data Out	t_{WD}		2.20	3.40	4.40	
Address to Match	t_{AM}		2.20	3.45	4.50	
Mask to Data	t_{MD}		2.10	3.30	4.25	
$\overline{WS}$ to Match	t_{WSM}		2.20	3.30	4.40	
Write Pulse Width	t_W	Fig. 1 t_W=1.20ns	1.20	0.80	—	
Address Set-up Before Write Time	t_{AS}		0.00	0.25	—	
Address Hold After Write Time	t_{AH}		0.00	0.30	—	
Data In Set-up Before Write Time	t_{DS}		−0.80	−1.25	—	
Data In Hold After Write Time	t_{DH}		0.50	0.20	—	
Mask In Hold to Inhibit Write Time	t_{MH}		1.10	0.71	—	
Mask In Set-up to Inhibit Write Time	t_{MS}		−0.40	−0.70	—	
Transition Time	t_{TLH}		0.50	1.10	2.00	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

■TIMING RELATIONSHIPS (t_W=1.20ns)

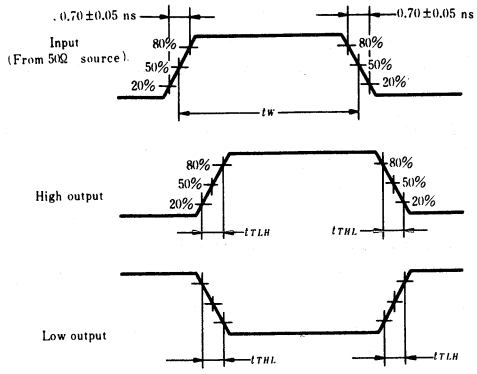


Fig.1 Output Rise and Fall Times and Waveforms

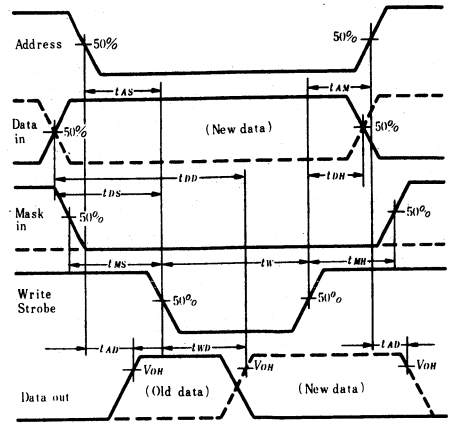


Fig.2 Write Mode and Read/Write Mode Waveforms

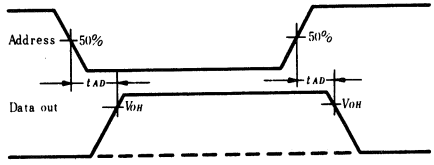


Fig.3 Read Mode Waveforms

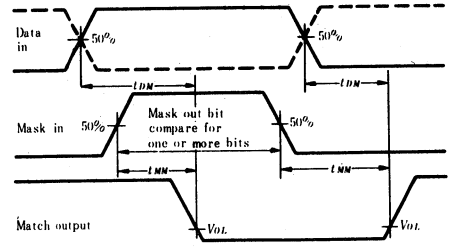


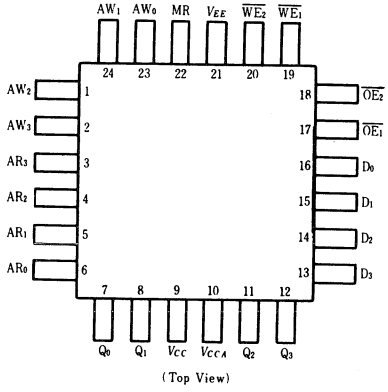
Fig.4 Search Mode Waveforms

HD100145F

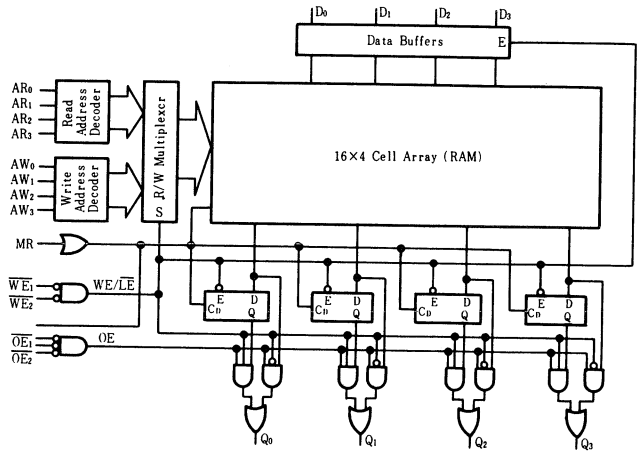
16×4 Read/Write Register File

The HD100145F is a 64-bit Register File organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting-up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the WRITE mode and the latches are in a HOLD mode. When either $\overline{WE}$ input is HIGH, the circuit is in the READ mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches and forces the outputs LOW.

■PIN ARRANGEMENT



■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			119	170	247	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	$\overline{WE}/\overline{LE}$ input		—	—	270	μA
			All input except $\overline{WE}/\overline{LE}$		—	—	220	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IL\ min}$		$R_L=50\Omega$,	−1025	−955	−880	mV
	V_{OL}			$V_{TT}=-2.0V$	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_L=50\Omega$,	−1035	—	—	mV
	V_{OLC}			$V_{TT}=-2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

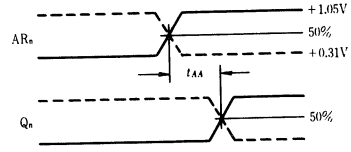
■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item		Symbol	Test Condition	min	typ	max	Unit
Access/ Recovery Timing	Address Access	t_{AA}	Fig. 1 a	2.00	5.50	7. 20	ns
	Output Recovery	t_{OR}	Fig. 1 b	1.00	2.20	2. 90	ns
	Output Disable	t_{OD}		1.00	2.20	2. 90	ns
Read Timing	Address Set-up	t_{RSA1}	Fig. 1 c	3.00	2.00	—	ns
	Output Delay	t_{WEQ}		2.00	4.50	5. 90	ns
Output Latch Timing	Address Set-up	t_{RSA2}	Fig. 1 d	8.30	5.50	—	ns
	Address Hold	t_{RHA}	Fig. 1 e	0.00	−2.00	—	ns
Write Timing	Address Set-up	t_{WSA}	Fig. 2 a	3.00	2.00	—	ns
	Address Hold	t_{WHA}		0.00	−1.30	—	ns
	Data Set-up	t_{WSD}		9.00	6.00	—	ns
	Data Hold	t_{WHD}		0.00	−1.20	—	ns
	Min. Write Pulse Width	t_W		6.00	4.00	—	ns
	$\overline{WE}$ to $\overline{WE}$ Set-up	t_{SW}	Fig. 2 b	0.50	—	—	ns
	$\overline{WE}$ to $\overline{WE}$ Hold	t_{HW}		0.00	—	—	ns
Master Reset Timing	Min. Reset Pulse Width	t_M	Fig. 3 a	4.30	—	—	ns
	$\overline{WE}$ Hold to Write	t_{MHW}		7.00	—	—	ns
	Output Disable	t_{MQ}	Fig. 3 b	3.50	—	—	ns

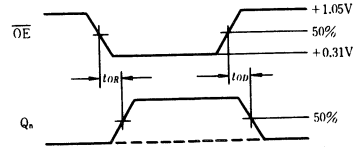
Not) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

■TIMING RELATIONSHIPS

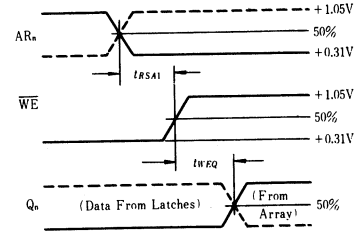
(a) Address Access Time
($\overline{WE}_1$, or $\overline{WE}_2$ = High : $\overline{OE}_1$ = $\overline{OE}_2$ = Low)



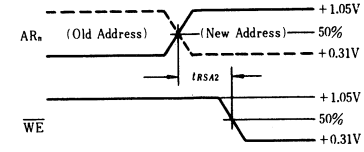
(b) Output Recovery/Disable Time
(unpulsed $\overline{OE}$ = Low)



(c) Read Timing, Address Set-up Time
(unpulsed $\overline{WE}$, $\overline{OE}_1$, $\overline{OE}_2$ = Low)



(d) Output Latch Timing, Address Set-up Time
(unpulsed $\overline{WE}$ = Low)



(e) Output Latch Timing, Address Hold Time
(unpulsed $\overline{WE}$ = Low)

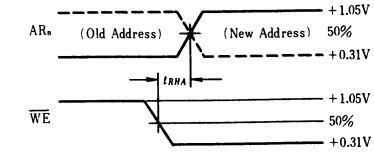
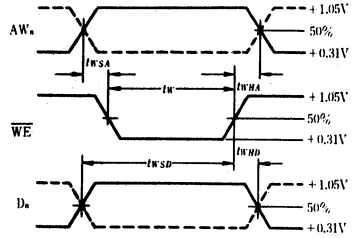


Fig.1 Read Timing

(a) Address and Data Set-up Time and Hold Time, Write Pulse Width (unpulsed $\overline{WE}$=Low)



(b) $\overline{WE}$ Set-up and hold times, write with other $\overline{WE}$

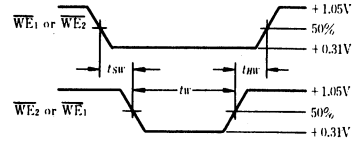
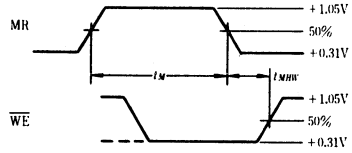


Fig.2 Write Timing

(a) Reset pulse width, $\overline{WE}$ hold time for subsequent writing (address already set-up, unpulsed $\overline{WE}$=Low)



(b) Output reset delay, MR to Q_n

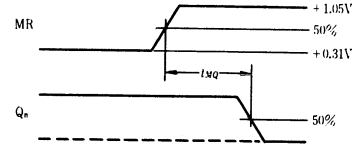


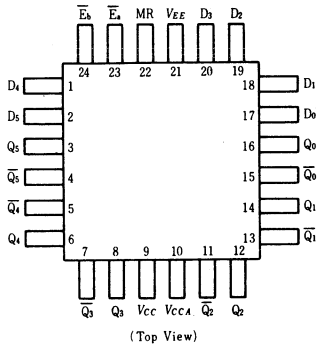
Fig.3 Master Reset Timing

HD100150F

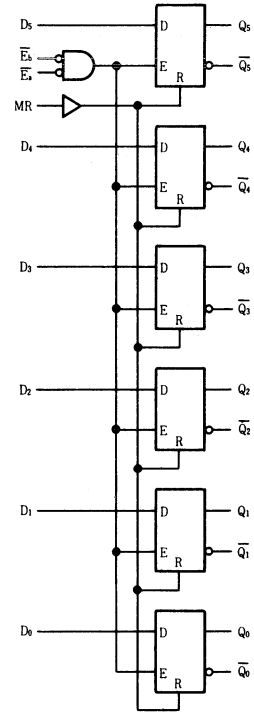
Hex D-type Latches

The HD100150F contains six D-type latches with the True and Complement Outputs, a pair of Common Enables ($\overline{Ea}$ and $\overline{Eb}$), and a Common Master Reset(MR). A Q output follows its D input when both $\overline{Ea}$ and $\overline{Eb}$ are low. When either $\overline{Ea}$ or $\overline{Eb}$ (or both) are high, a latch stores the last valid data present on its D input before $\overline{Ea}$ or $\overline{Eb}$ went high. The MR input overrides all other inputs and makes the Q outputs low.

■PIN ARRANGEMENT



(Top View)



■TRUTH TABLE (each latch)

Dn	$\overline{Ea}$	$\overline{Eb}$	MR	Qn
L	L	L	L	L
H	L	L	L	H
×	H	×	L	*
×	×	H	L	*
×	×	×	H	L

H = High Level
L = Low Level
× = Immaterial
* = Retains data present before $\overline{E}$ positive transition

■DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		79	113	159	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\,max}$	MR input	—	—	450	μA
			Data input	—	—	340	μA
			Enable input	—	—	520	μA
	I_{IL}	$V_{IN}=V_{IL\,min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\,max}$ or $V_{IL}=V_{IL\,min}$	$R_L=50\Omega$, $V_{TT}=-2.0V$	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\,min}$ or $V_{IN}=V_{IL\,max}$	$R_L=50\Omega$, $V_{TT}=-2.0V$	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	Fig. 1	Enable input	0.75	1.15	1.50	ns
			MR input	1.15	1.85	2.50	
			Data input	0.55	0.85	1.20	
Transition Time	t_{TLH}, t_{THL}			0.45	0.90	1.50	ns
Set-up Time	t_{su}	Fig. 2	Data input	0.60	—	—	ns
			MR input (Release Time)	2.00	—	—	
Hold Time	t_h		Data input	0.30	—	—	ns
Pulse Width	t_{PW}		$\overline{E}$ (Low)	0.75	—	—	ns
			MR (High)	1.30	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

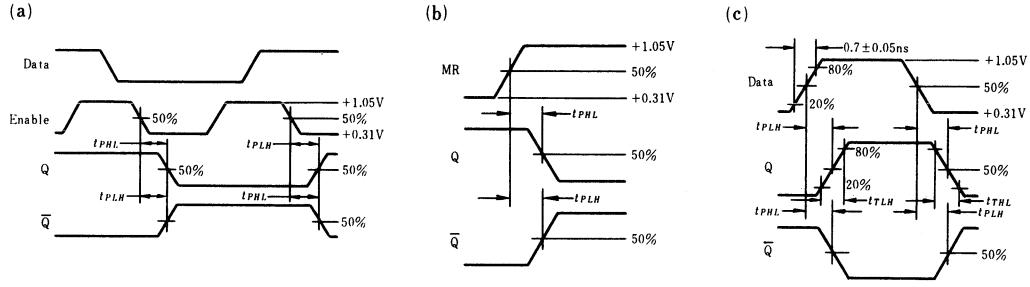


Fig.1 Propagation Delay Time

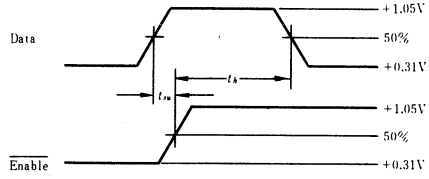


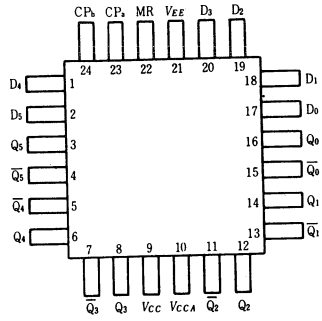
Fig.2 Set-up and Hold Time

HD100151F

Hex D-type Flip-Flops

HD100151F contains six master/slave flip-flops with True and Complement outputs. A pair of Common Clock inputs (CPa and CPb) and common Master Reset (MR) input. Data enters a master when both CPa and CPb are low and transfers to the slave when CPa or CPb (or both) go high. The MR inputs overrides all other inputs and makes the Q outputs low.

■PIN ARRANGEMENT



(Top View)

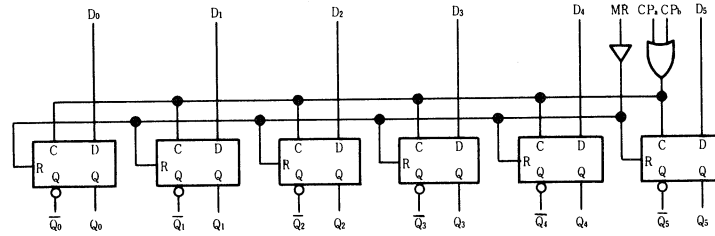
■TRUTH TABLE (Each Flip Flop)

D_n	CP_a	CP_b	MR	$Q_{n(t+1)}$
L	⎍	L	L	L
H	⎍	L	L	H
L	L	⎍	L	L
H	L	⎍	L	H
×	H	⎍	L	$Q_{n(t)}$
×	⎍	H	L	$Q_{n(t)}$
×	×	×	H	L

× : Immaterial

t, t+1 : Time before and after CP positive transition

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		98	141	198	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\,max}$	MR input	—	—	450	μA
			$D_0\sim D_5$ input	—	—	225	
			CP_a, CP_b input	—	—	520	
	I_{IL}	$V_{IN}=V_{IL\,min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\,max}$ or $V_{IN}=V_{IL\,min}$	$R_T=50\Omega$, $V_{TT}=-2.0V$	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\,min}$ or $V_{IN}=V_{IL\,max}$	$R_T=50\Omega$, $V_{TT}=-2.0V$	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See Test Circuit and Waveform	CP input	0.80	1.30	1.80	ns
			MR input	1.20	1.85	2.50	
Transition Time	t_{TLH} t_{THL}			0.40	0.90	1.20	ns
Toggle Frequency	f_{tog}			400	550	—	MHz
Set-up Time	t_{su}		D input	0.60	—	—	ns
			MR input (Release Time)	2.00	—	—	
Hold Time	t_h		D input	−0.20	—	—	ns
Pulse Width	t_{pw}		CP (High)	1.10	—	—	ns
			MR (High)	1.30	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

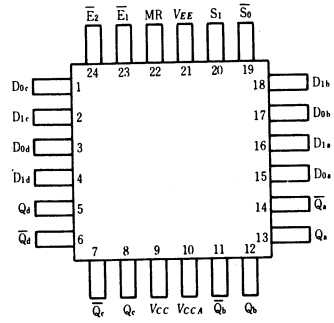
HD100155F

Quad. Multiplexers/Latches

The HD100155F contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{En}$) inputs are low, the data that appears at an output is controlled by the Select (Sn) inputs, as shown in the operating mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs low for the case where the latch is transparent (both Enables are low) and can steer a high signal from either D_0 or D_1 to an output. The Select inputs can be tied togehter for applications requiring only that data be steered from either D_0 or D_1.

A positive-going signal on either Enable input latches the outputs. A high signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs low.

■PIN ARRANGEMENT



(Top View)

■OPERATING MODE TABLE

CONTROLS				OUTPUT
$\overline{E_1}$	$\overline{E_2}$	$\overline{S_0}$	S_1	Q_n
H	×	×	×	latched*
×	H	×	×	latched*
L	L	L	L	D_{0n}
L	L	L	H	$D_{0n}+D_{1n}$
L	L	H	L	L
L	L	H	H	D_{1n}

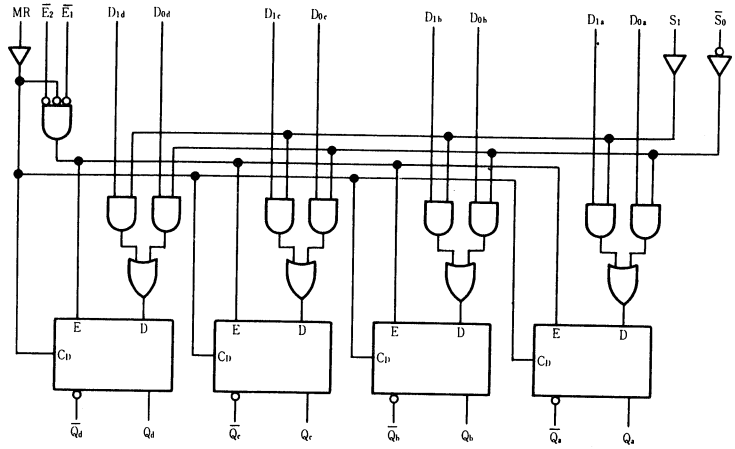
H = High Level
L = Low Level
× = immaterial
* = Stores data present before $\overline{E}$ went high.

■TRUTH TABLE

Input							Output	
MR	$\overline{E_1}$	$\overline{E_2}$	S_1	$\overline{S_0}$	D_{1a} D_{1b} D_{1c} D_{1d}	D_{0a} D_{0b} D_{0c} D_{0d}	$\overline{Q_a}$ $\overline{Q_b}$ $\overline{Q_c}$ $\overline{Q_d}$	Q_a Q_b Q_c Q_d
H	×	×	×	×	×	×	H	L
L	L	L	H	H	H	×	L	H
L	L	L	H	H	L	×	H	L
L	L	L	L	L	×	H	L	H
L	L	L	L	L	×	L	H	L
L	L	L	L	H	×	×	H	L
L	L	L	H	L	H	×	L	H
L	L	L	H	L	×	H	L	H
L	L	L	H	L	L	L	H	L
L	H	×	×	×	×	×	No Change	
L	×	H	×	×	×	×	No Change	

H = High level
L = Low Level
× = Immaterial

■LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			66	95	133	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	S_n input		—	—	220	μA
			$\overline{E}_n$ input		—	—	350	
			Data input		—	—	340	
			MR input		—	—	430	
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		R_T = 50Ω, V_{TT} = −2.0V	−1025	−955	−880	mV
	V_{OL}				−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		R_T = 50Ω, V_{TT} = −2.0V	−1035	—	—	mV
	V_{OLC}				—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See Test Circuit and Waveform	Data input	0.70	1.20	1.55	ns
			S input	1.50	2.50	3.25	
			$\overline{E}$ input	1.00	1.70	2.20	
			MR input	1.00	1.85	2.70	
Transition Time	t_{TLH} t_{THL}			0.50	1.10	1.65	ns
Set-up Time	t_{su}		Data input	0.60	—	—	ns
			S input	2.30	—	—	
			MR input (Release Time)	1.40	—	—	
Hold Time	t_h		Data input	0.30	—	—	ns
			S input	−0.50	—	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) in maintained.

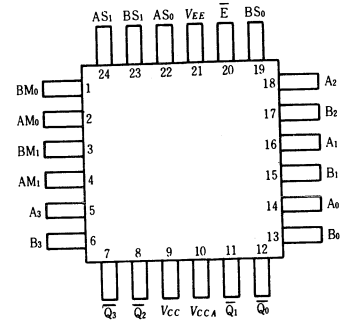
Mask-merge

The HD100156F merges two 4-bit words to form a 4-bit output word. The AMj enable allows the merge of An into Bn by one, two, or three places (per the ASj value) from the left. The BMj enable similarly allows the merge of Bn into An from the left (per the BSj value). The Bn merge overrides the An merge when both are enabled.

This means An first merges into Bn and Bn then merges into the An merge. A Bn address (BSj) greater than or equal to the An address (ASj) thus forces the outputs to all Bn. The merge outputs feed 4 latches, which have a common enable ($\overline{E}$) input. All inputs have a 50kΩ (typ.) pull-down resistor tied to V_{EE}.

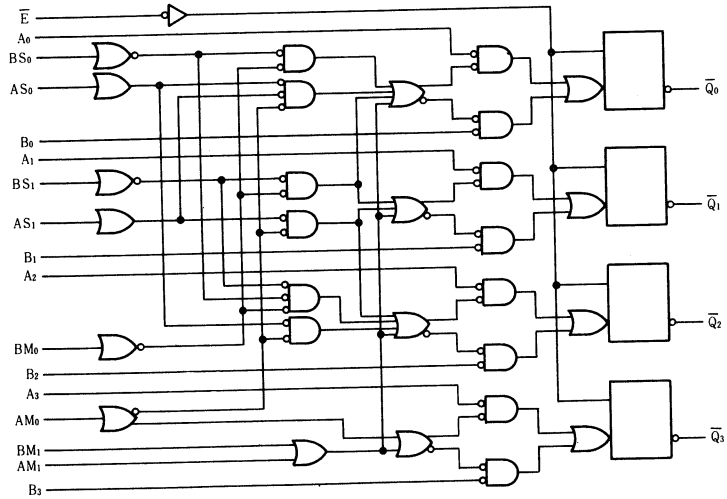
All four outputs do not have pull-down resistors, so they have wired-OR capability and will require external resistors.

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■TRUTH TABLE

Input									Output				
BM_1	BM_0	AM_1	AM_0	BS_1	BS_0	AS_1	AS_0	$\overline{E}$	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	
×	×	H	×	×	×	×	×	L	B_0	B_1	B_2	B_3	
H	×	×	×	×	×	×	×	L	B_0	B_1	B_2	B_3	
L	L	L	L	×	×	×	×	L	A_0	A_1	A_2	A_3	
L	L	L	H	×	×	L	L	L	B_0	B_1	B_2	B_3	
L	L	L	H	×	×	L	H	L	A_0	B_1	B_2	B_3	
L	L	L	H	×	×	H	L	L	A_0	A_1	B_2	B_3	
L	L	L	H	×	×	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	×	×	L	A_0	A_1	A_2	A_3	
L	H	L	L	L	H	×	×	L	B_0	A_1	A_2	A_3	
L	H	L	L	H	L	×	×	L	B_0	B_1	A_2	A_3	
L	H	L	L	H	H	×	×	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	L	L	B_0	A_1	B_2	B_3	
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	B_3	
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	ADDRESS (BS) > ADDRESS (AS)
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
×	×	×	×	×	×	×	×	H	Q_0	Q_1	Q_2	Q_3	

H = High Level
L = Low Level
× = Don't care

■DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		107	153	214	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	BS_i, AS_i, $\overline{E}$, BM_j, AM_j	—	—	265	μA
			A_n, B_n	—	—	340	
	I_{IL}	$V_{IN} = V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$	R_T = 50Ω, V_{TT} = −2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$	R_T = 50Ω, V_{TT} = −2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See Test Circuit and Waveforms	A_n, B_n	0.70	1.20	1.80	ns
			$\overline{E}$	1.40	2.00	2.70	
			Address	1.60	2.60	3.70	
			AM_j, BM_j	1.60	2.70	4.00	
Transition Time	t_{TLH} t_{THL}			0.50	0.90	2.50	ns
Set-up Time	t_{su}		Data	0.00	—	—	ns
			AM_j, BM_j	1.80	—	—	
			AS_j, BS_j	1.80	—	—	
Hold Time	t_h		Data	1.50	—	—	ns
			AM_j, BM_j	−0.50	—	—	
			AS_j, BS_j	−0.50	—	—	
Pulse Width	t_{PW}		$\overline{E}$(Low)	1.40	—	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

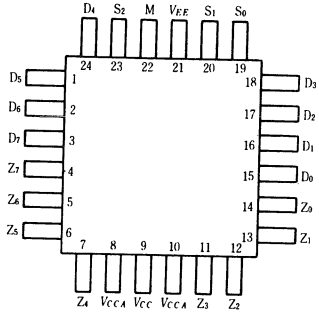
8-bit Shift Matrix

The HD100158F contains a combinatorial network which performs the function of an 8-bit shift matrix. Three control lines (Sn) are internally decoded and define the number of places which an 8-bit word present at the inputs (Dn) is shifted to the left and presented at the outputs (Zn). A Mode Control input (M) is provided which if low, forces low all outputs to the right of the one that contain D_7. This operation is sometimes referred to as "low backfill".

If M is high, an end-round shift is performed such that D_0 appears at the output to the right of the one that contains D_7.

This operation is commonly referred to as "barrel shifting".

■PIN ARRANGEMENT



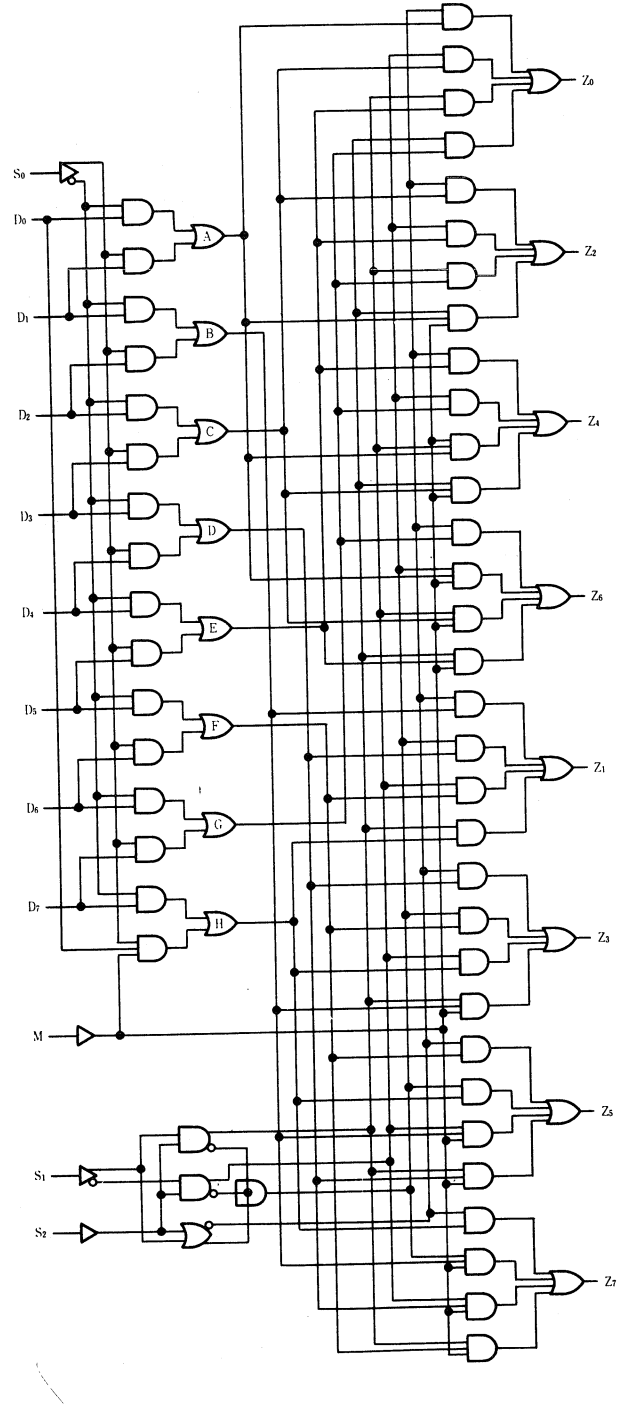
(Top View)

■TRUTH TABLE

INPUT				OUTPUT							
M	S_0	S_1	S_2	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
×	L	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
L	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L
L	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	L	L
L	H	H	L	D_3	D_4	D_5	D_6	D_7	L	L	L
L	L	L	H	D_4	D_5	D_6	D_7	L	L	L	L
L	H	L	H	D_5	D_6	D_7	L	L	L	L	L
L	L	H	H	D_6	D_7	L	L	L	L	L	L
L	H	H	H	D_7	L	L	L	L	L	L	L
H	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0
H	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1
H	H	H	L	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2
H	L	L	H	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3
H	H	L	H	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4
H	L	H	H	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5
H	H	H	H	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6

H = High level
L = Low level
× = Immaterial

LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		84	120	168	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$		—	—	220	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$	R_T = 50Ω	−1025	−955	−880	mV
	V_{OL}		V_{TT} = −2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$	R_T = 50Ω	−1035	—	—	mV
	V_{OLC}		V_{TT} = −2.0V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	D input	1.00	1.70	2.40	ns
	t_{PHL}		M input	1.25	2.30	3.80	
			S_n input	1.50	2.30	3.70	
Transition Time	t_{TLH}			0.50	1.30	2.20	ns
	t_{THL}						

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

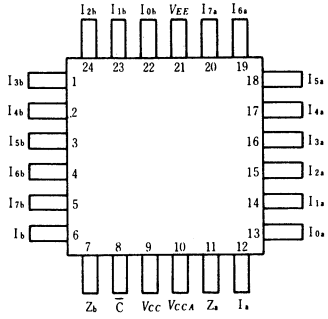
HD100160F

Dual Parity Generators/Checkers

The HD100160F is a Dual Parity Checker/Generator. Each half has nine inputs, with the output being high when an even number of inputs are high. One of the nine inputs (Ia or Ib) has the shorter (through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits. The HD100160F also has a Compare($\overline{C}$) output which allows the circuit to compare two 8-bit words.

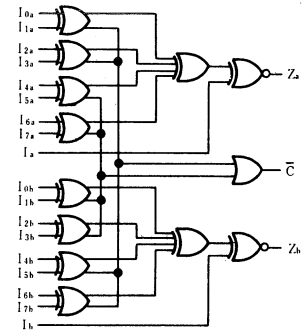
The $\overline{C}$ output is low when the two words match, bit for bit.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE (each half)

Sum of High Input	Output Z
EVEN	H
ODD	L

$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$

■ DC CHARACTERISTICS ($V_{EE} = -4.5V$, $V_{CC} = GND$, $Ta = 0 \sim +85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			57	82	115	mA
Input Current	I_H	$V_{IN} = V_{IH\ max}$	Ib, Ia		—	—	340	μA
			All input except Ib and Ia		—	—	220	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or $V_{IN} = V_{IL\ min}$		$R_L = 50\Omega$	−1025	−955	−880	mV
	V_{OL}			$V_{TT} = -2.0V$	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or $V_{IN} = V_{IL\ max}$		$R_L = 50\Omega$	−1035	—	—	mV
	V_{OLC}			$V_{TT} = -2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS ($V_{EE} = -2.5V$, $V_{CC} = 2.0V$, $Ta = 25°C$)

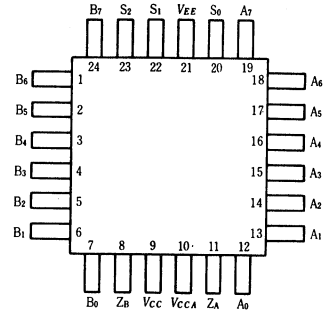
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	Ina, Inb to Z	1.30	2.50	3.75	ns
			Ina, Inb to $\overline{C}$	1.20	2.00	2.90	ns
			Ia, Ib to Z	0.60	0.90	1.40	ns
Transition Time	t_{TLH} t_{THL}			0.40	0.90	1.40	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Dual 8-input Multiplexers

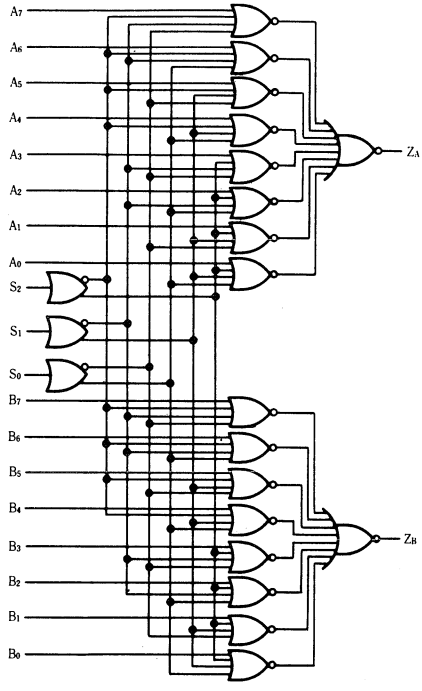
The HD100163F is a dual 8-input Multiplexer. The Data Select(Sn) inputs determine which bit (An and Bn) will be presented at the Outputs (Z_A and Z_B respectively). The same bit (0–7) will be selected for both the Z_A and Z_B output.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Input										Output
Address			Data							
S_2	S_1	S_0	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	
L L	L L	L L	×	×	×	×	×	×	×	L H	L H
L L	L L	H H	×	×	×	×	×	×	L H	×	L H
L L	H H	L L	×	×	×	×	×	L H	×	×	L H
L L	H H	H H	×	×	×	×	L H	×	×	×	L H
H H	L L	L L	×	×	×	L H	×	×	×	×	L H
H H	L L	H H	×	×	L H	×	×	×	×	×	L H
H H	H H	L L	×	L H	×	×	×	×	×	×	L H
H H	H H	H H	L H	×	×	×	×	×	×	×	L H

■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		76	109	153	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	S_n input	—	—	265	μA
			A_n, B_n input	—	—	340	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	R_L=50Ω	−1025	−955	−880	mV
	V_{OL}		V_{TT}=−2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	R_L=50Ω	−1035	—	—	mV
	V_{OLC}		V_{TT}=−2.0V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

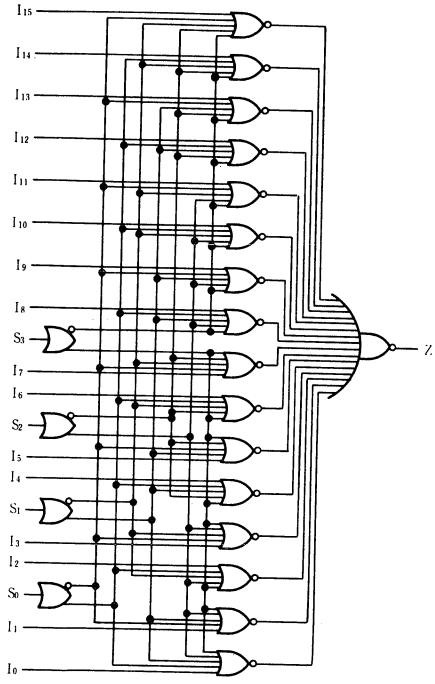
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveforms	Data input	0.60	0.95	1.50	ns
	t_{PHL}		Select input	1.10	1.75	2.50	
Transition Time	t_{TLH}			0.55	1.20	1.70	ns
	t_{THL}						

Note) The circuit in a test socket or mounted on a printed circuitboard and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained,

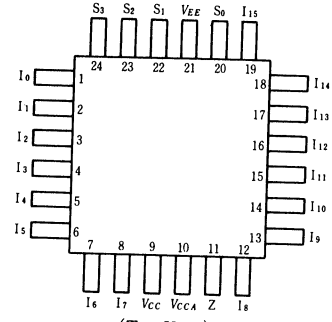
16-input Multiplexers

The HD100164F is a 16-input Multiplexer. Data paths are controlled by four select lines (S0–S3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data.

■ LOGIC DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		43	70	98	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	I_n input	—	—	280	μA
			S_0, S_1 input	—	—	240	μA
			S_2, S_3 input	—	—	200	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	R_L=50Ω	−1025	−955	−880	mV
	V_{OL}		V_{TT}=−2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	R_L=50Ω	−1035	—	—	mV
	V_{OLC}		V_{TT}=−2.0V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	I_n input	1.00	1.65	2.35	ns
			S_0, S_1 input	1.45	2.40	3.20	
			S_2, S_3 input	1.10	1.85	2.55	
Transition Time	t_{TLH} t_{THL}			0.50	1.00	1.60	ns

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5 m/s (500 linear fpm) is maintained.

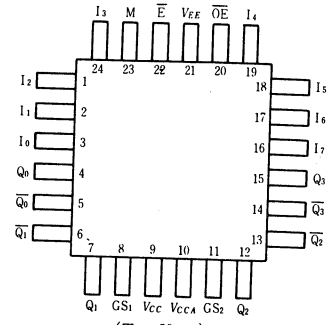
Universal Priority Encoders

The HD100165F contains eight input latches with a Common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a high signal. The circuit operates as a dual 4-input encoder when the Mode Control input (M) is low, and as a single 8-input encoder when M is high.

In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with I_0-I_3. Q_2, Q_3 and GS_2 operate with I_4-I_7.

A GS output goes low when its pertinent inputs are all low. Inputs are latched when $\overline{E}$ goes high. A high signal on the Output Enable ($\overline{OE}$) input forces all Q outputs low and GS outputs high. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group.

■ PIN ARRANGEMENT



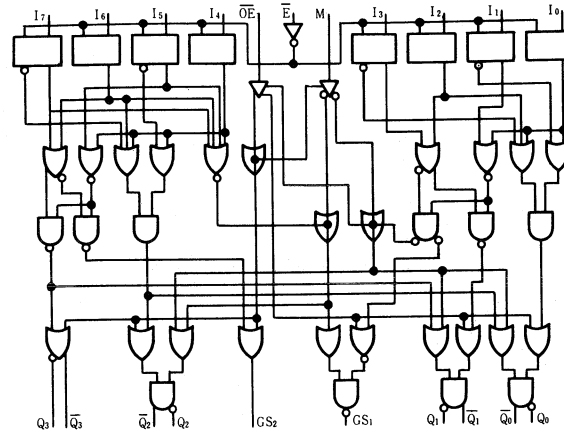
(Top View)

■ TRUTH TABLE

$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	×	×	×					L	L			H	
L	L	L	L	H	×	×					H	L			H	
L	L	L	L	L	H	×					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	×	×	×			L	L		H
L	L	L					L	H	×	×			H	L		H
L	L	L					L	L	H	×			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	×	×	×	×	×	×	×	L	L	L	L	H	H
L	L	H	L	H	×	×	×	×	×	×	H	L	L	L	H	H
L	L	H	L	L	H	×	×	×	×	×	L	H	L	L	H	H
L	L	H	L	L	L	H	×	×	×	×	H	H	L	L	H	H
L	L	H	L	L	L	L	H	×	×	×	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	×	×	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	×	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
×	H	×	×	×	×	×	×	×	×	×	L	L	L	L	H	H
H	L	L	×	×	×	×	×	×	×	×	*	*	*	*	*	*
H	L	H	×	×	×	×	×	×	×	×	*	*	*	*	*	*

H = High Level
L = Low Level
* = Stores data present before $\overline{E}$ went high.

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		77	110	154	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$		—	—	230	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_T=50\Omega$, $V_{TT}=-2.0V$	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_T=50\Omega$, $V_{TT}=-2.0V$	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■AC CHARACTERISTICS ($V_{EE}=-2.5V$, $V_{CC}=2.0V$, $Ta=25°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	Fig. 1	In→Qn, $\overline{Qn}$	1.10	2.15	3.35	ns
			In→GS_1, GS_2	1.00	2.00	3.35	
			$\overline{E}$→Qn, $\overline{Qn}$	1.75	3.00	3.80	
			$\overline{E}$→GS_1, GS_2	1.75	3.00	3.80	
			$\overline{OE}$→Qn, $\overline{Qn}$	1.00	1.75	2.50	
			$\overline{OE}$→GS_1, GS_2	1.00	1.80	2.65	
			M→Qn, $\overline{Qn}$	1.00	2.00	3.00	
			M→GS_1, GS_2	1.00	2.00	3.00	
Transition Time	t_{TLH} t_{THL}	Fig. 1		0.40	0.90	1.30	ns
Set-up Time	t_{su}	Fig. 2	In input	0.60	—	—	ns
Hold Time	t_h			0.40	—	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

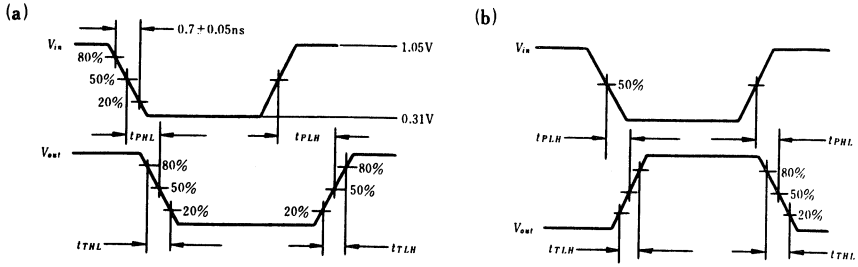


Fig.1 Propagation Delay Time

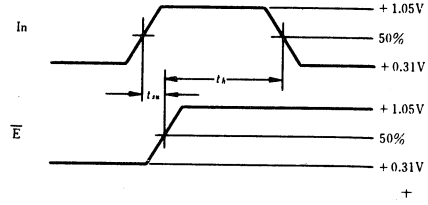


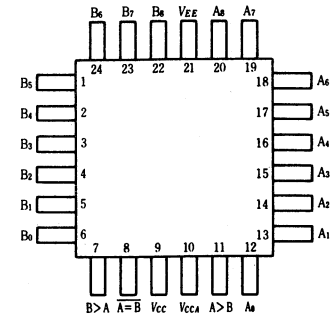
Fig. 2 Set-up and Hold Time

9-bit Comparators

The HD100166F is a 9-bit Magnitude Comparator which compares the arithmetic value of two 9-bit words and indicates whether one word is greater than, or equal to the other.

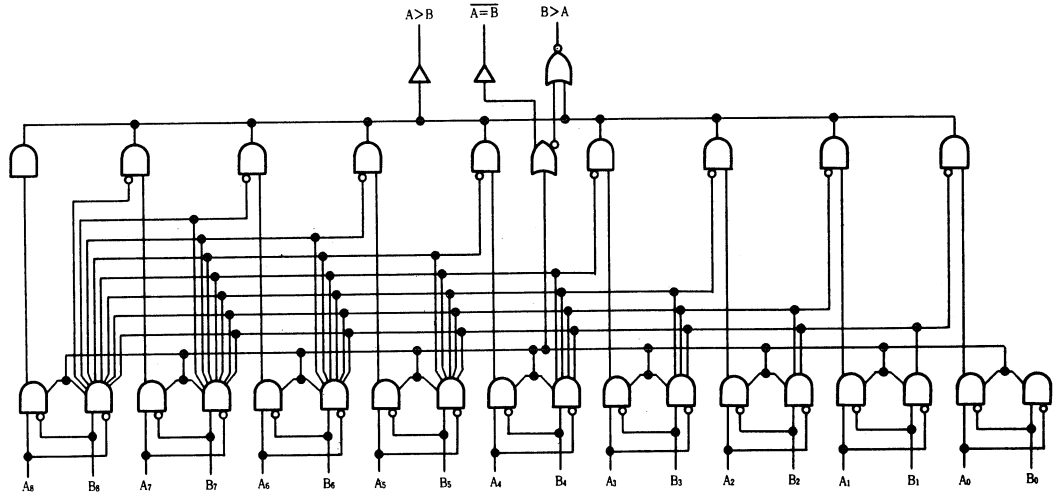
The outputs do not have pull down resistors, which provides the wire OR functions by tying several outputs together.

■PIN ARRANGEMENT



(Top View)

■LOGIC DIAGRAM



■ TRUTH TABLE

Input										Output		
A_8 B_8	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	A>B	B>A	$\overline{A=B}$
H L									H	L	H
L H									L	H	H
$A_8=B_8$	H L								H	L	H
$A_8=B_8$	L H								L	H	H
$A_8=B_8$	$A_7=B_7$	H L							H	L	H
$A_8=B_8$	$A_7=B_7$	L H							L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	H L						H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	L H						L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	H L					H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	L H					L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	H L				H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	L H				L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	H L			H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	L H			L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	H L		H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	L H		L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	H L	H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	L H	L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L

H=High Level
L=Low Level
Blank=Don't care

■ DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0\sim+85$°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		119	170	238	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$		—	—	250	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_T=50\Omega$,	−1025	−955	−880	mV
	V_{OL}		$V_{TT}=-2.0$V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_T=50\Omega$,	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0$V	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS ($V_{EE}=-2.5$V, $V_{CC}=2.0$V, $Ta=25$°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	See test circuit and waveform	1.20	2.10	3.00	ns
	t_{PHL}					
Transition Time	t_{TLH}		0.45	0.90	1.30	ns
	t_{THL}					

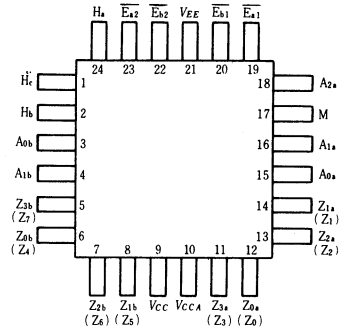
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5 m/s (500 linear fpm) is maintained.

HD100170F

Universal Demultiplexers/Decoders

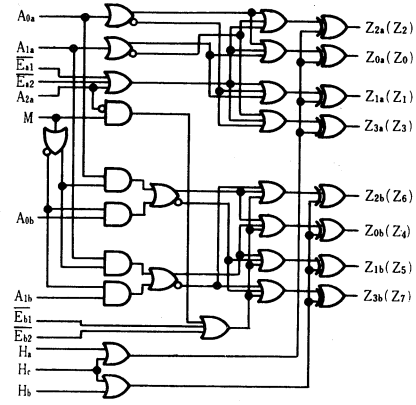
The HD100170F Universal Demultiplexer/Decoder functions as either a dual Mode Control input(M). In the dual mode, each half has a pair of active low Enable($\overline{E}$) inputs. Pin assignments for the $\overline{E}$ inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active low enables (pin 19 to 20 and pin 22 to 23). Signals applied to auxiliary inputs Ha, Hb and Hc determine whether the outputs are active high or active low. In the dual 1-of-4 mode the address inputs are A0a, A1a and A0b, A1b with A2a unused (i.e., left open, tied to V_{BB} or with low signal applied). In the 1-of-8 mode, the address inputs are A0a, A1a, A2a with A0b and A1b low or open.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



(Zn) for 1-of-8 applications

■ TRUTH TABLE

● Dual 1-of-4 Mode ($M = A_{2a} = H_C = L$)

Input				Active High Output ($H_a, H_b = H$)				Active Low Output ($H_a, H_b = L$)			
$\overline{E_{a1}}$	$\overline{E_{a2}}$	A_{1a}	A_{0a}	Z_{0a}	Z_{1a}	Z_{2a}	Z_{3a}	Z_{0a}	Z_{1a}	Z_{2a}	Z_{3a}
$\overline{E_{b1}}$	$\overline{E_{b2}}$	A_{1b}	A_{0b}	Z_{0b}	Z_{1b}	Z_{2b}	Z_{3b}	Z_{0b}	Z_{1b}	Z_{2b}	Z_{3b}
H	×	×	×	L	L	L	L	H	H	H	H
×	H	×	×	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

● Single 1-of-8 Mode ($M = H : A_{0b} = A_{1b} = H_a = H_b = L$)

Input					Active High Output ($H_C = H$)*							
$\overline{E_1}$	$\overline{E_2}$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	×	×	×	×	L	L	L	L	L	L	L	L
×	H	×	×	×	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

* for H_C=Low, Output states are complemented.
$E_1 = E_{a1} \cdot E_{b1}$, $E_2 = E_{a2} \cdot E_{b2}$

■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			76	109	153	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	H_c, A_{0}, A_{1a}, A_{2a} input		—	—	310	μA
			All other input		—	—	250	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		R_L=50Ω,	−1025	−955	−880	mV
	V_{OL}			V_{TT}=−2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		R_L=50Ω	−1035	—	—	mV
	V_{OLC}			V_{TT}=−2.0V	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	$\overline{E}_a/\overline{E}_b$ input	0.90	1.35	1.80	ns
			A input	0.90	1.60	2.30	ns
			H input	1.00	1.75	2.50	ns
			M input	1.60	2.60	3.60	ns
Transition Time	t_{TLH} t_{THL}			0.50	1.00	1.60	ns

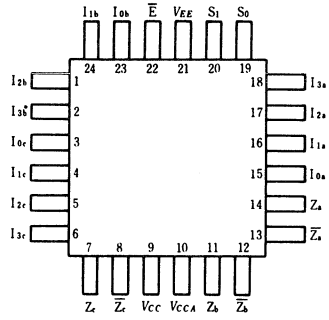
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5 m/s (500 linear fpm) is maintained.

HD100171F

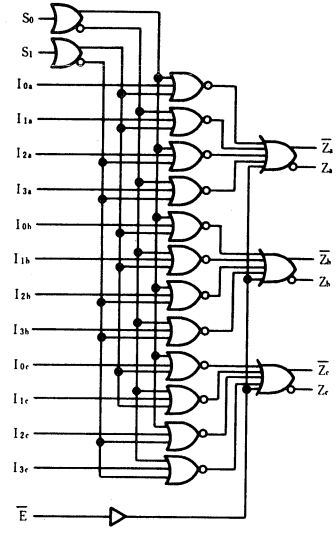
Triple 4-input Multiplexers with Enable

The HD100171F contains Triple 4-input multiplexers which share a common decoder (inputs S0 and S1). Output buffer gates provide true and complement outputs. A high on the Enable input ($\overline{E}$) forces all true outputs low (see truth table).

■ PIN ARRANGEMENT



■ LOGIC DIAGRAM



■ TRUTH TABLE

$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0n}
L	H	L	I_{1n}
L	L	H	I_{2n}
L	H	H	I_{3n}
H	×	×	L

■ DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			56	81	114	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	S_0, S_1, $\overline{E}$ input		—	—	300	μA
			Data input		—	—	340	μA
	I_{IL}	$V_{IN}=V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$		$R_L=50\Omega$	−1025	−955	−880	mV
	V_{OL}			$V_{TT}=-2.0V$	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$		$R_L=50\Omega$	−1035	—	—	mV
	V_{OLC}			$V_{TT}=-2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS ($V_{EE}=-2.5V$, $V_{CC}=2.0V$, $Ta=25°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	Data input	0.55	0.95	1.30	ns
			S_0/S_1 input	1.00	1.60	2.30	ns
			$\overline{E}$ input	0.90	1.50	2.10	ns
Transition Time	t_{TLH}, t_{THL}			0.45	0.90	1.35	ns

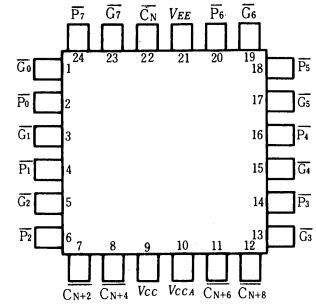
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5 m/s (500 linear fpm) is maintained.

HD100179F

Carry Look-ahead

The HD100179F is a high speed carry look-ahead general intended for use with the HD100180F 6-bit fast Adder and the HD100181F 4-bit ALU.

■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

● $\overline{C_{N+2}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{C_{N+2}}$
×	×	×	L	×	L
×	L	×	×	L	L
L	×	L	×	L	L
All other combinations					H

$\overline{C_{N+2}} = \overline{G_1} \cdot (\overline{P_1} + \overline{G_0}) \cdot (\overline{P_1} + \overline{P_0} + \overline{C_N})$

× = Don't care

● $\overline{C_{N+4}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	$\overline{C_{N+4}}$
×	×	×	×	×	×	×	L	×	L
×	×	×	×	×	L	×	×	L	L
×	×	×	L	×	×	L	×	L	L
×	L	×	×	L	×	L	×	L	L
L	×	L	×	L	×	L	×	L	L
All other combinations									H

$\overline{C_{N+4}} = \overline{G_3} \cdot (\overline{P_3} + \overline{G_2}) \cdot (\overline{P_3} + \overline{P_2} + \overline{G_1}) \cdot (\overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0}) \cdot (\overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{P_0} + \overline{C_N})$

● $\overline{C_{N+6}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	$\overline{G_4}$	$\overline{P_4}$	$\overline{G_5}$	$\overline{P_5}$	$\overline{C_{N+6}}$
×	×	×	×	×	×	×	×	×	×	×	L	×	L
×	×	×	×	×	×	×	×	×	L	×	×	L	L
×	×	×	×	×	×	×	L	×	×	L	×	L	L
×	×	×	×	×	L	×	×	L	×	L	×	L	L
×	×	×	L	×	×	L	×	L	×	L	×	L	L
×	L	×	×	L	×	L	×	L	×	L	×	L	L
L	×	L	×	L	×	L	×	L	×	L	×	L	L
All other combinations													H

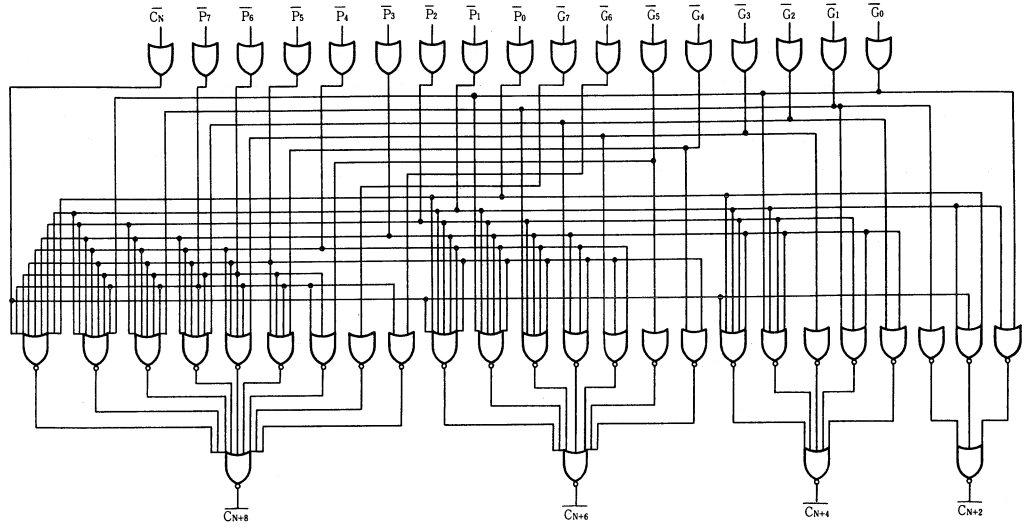
$\overline{C_{N+6}} = \overline{G_5} \cdot (\overline{P_5} + \overline{G_4}) \cdot (\overline{P_5} + \overline{P_4} + \overline{G_3}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{G_2}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{G_1}) \cdot$
$(\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{P_0} + \overline{C_N})$

● $\overline{C_{N+8}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	$\overline{G_4}$	$\overline{P_4}$	$\overline{G_5}$	$\overline{P_5}$	$\overline{G_6}$	$\overline{P_6}$	$\overline{G_7}$	$\overline{P_7}$	$\overline{C_{N+8}}$
×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	L	×	L
×	×	×	×	×	×	×	×	×	×	×	×	×	L	×	×	L	L
×	×	×	×	×	×	×	×	×	×	×	L	×	×	L	×	L	L
×	×	×	×	×	×	×	×	×	L	×	×	L	×	L	×	L	L
×	×	×	×	×	×	×	L	×	×	L	×	L	×	L	×	L	L
×	×	×	×	×	L	×	×	L	×	L	×	L	×	L	×	L	L
×	×	×	L	×	×	L	×	L	×	L	×	L	×	L	×	L	L
×	L	×	×	L	×	L	×	L	×	L	×	L	×	L	×	L	L
L	×	L	×	L	×	L	×	L	×	L	×	L	×	L	×	L	L
All other combinations																	H

$\overline{C_{N+8}} = \overline{G_7} \cdot (\overline{P_7} + \overline{G_6}) \cdot (\overline{P_7} + \overline{P_6} + \overline{G_5}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{G_4}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{G_3}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{G_2}) \cdot$
$(\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{G_1}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{P_0} + \overline{C_N})$

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		115	165	231	mA
Input Current	I_{IH}	$V_{IH}=V_{IH}$ max	$\overline{Gn}$ input	—	—	250	μA
			$\overline{Pn}$ input	—	—	340	
	I_{IL}	$V_{IH}=V_{IL}$ min		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ max or $V_{IN}=V_{IL}$ min	R_T=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH}$ min or $V_{IN}=V_{IH}$ max	R_T=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	1.10	1.80	2.45	ns
Transition Time	t_{TLH}, t_{THL}		0.40	1.00	1.50	ns

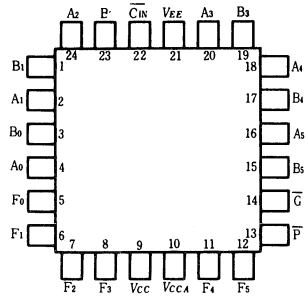
Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100180F

Fast 6-bit Adders

The HD100180F is a High Speed 6-bit Adder capable of performing as full 6-bit addition of 2 operands in 2ns.
Inputs for the adder are active low Carry-In. Operand A, and Operand B; outputs are Function, active low Carry Generate, and active low Carry Propagate. When used with the HD100179F, Full Carry Lookahead, as a second order Lookahead Block. HD100180F provides high speed addition of very long words.

■ PIN ARRANGEMENT

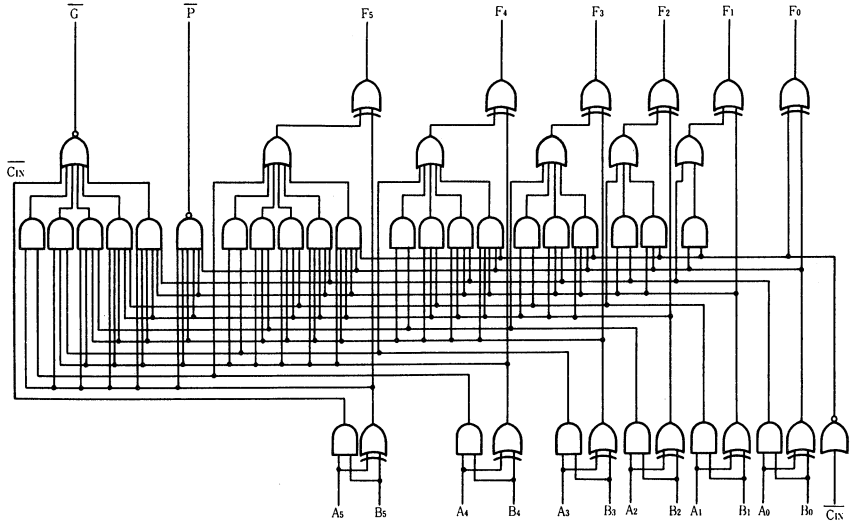


(Top View)

■ LOGIC FUNCTION

$$F_0 = P_0 \oplus C_{IN}$$
$$F_1 = P_1 \oplus (G_0 + P_0 C_{IN})$$
$$F_2 = P_2 \oplus (G_1 + P_1 G_0 + P_1 P_0 C_{IN})$$
$$F_3 = P_3 \oplus (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{IN})$$
$$F_4 = P_4 \oplus (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{IN})$$
$$F_5 = P_5 \oplus (G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 G_0 + P_4 P_3 P_2 P_1 P_0 C_{IN})$$
$$\overline{P} = \overline{P_0 P_1 P_2 P_3 P_4 P_5}$$
$$\overline{G} = \overline{G_5 + P_5 G_4 + P_5 P_4 G_3 + P_5 P_4 P_3 G_2 + P_5 P_4 P_3 P_2 G_1 + P_5 P_4 P_3 P_2 P_1 G_0}$$
$$P_0 = A_0 \oplus B_0$$
$$P_1 = A_1 \oplus B_1$$
$$P_2 = A_2 \oplus B_2$$
$$P_3 = A_3 \oplus B_3$$
$$P_4 = A_4 \oplus B_4$$
$$P_5 = A_5 \oplus B_5$$

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		137	195	255	mA
Input Current	I_{IH}	$V_{IN}=V_{IH}$ max		—	—	220	μA
	I_{IL}	$V_{IN}=V_{IL}$ min		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ max or $V_{IN}=V_{IL}$ min	R_T=50Ω, V_{TT}=−2.0V	−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH}$ min or $V_{IN}=V_{IL}$ max	R_T=50Ω, V_{TT}=−2.0V	−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	An/Bn→Fn	1.20	2.25	3.35	ns
			An/Bn→Pn	1.00	1.90	2.75	
			An/Bn→Gn	1.30	2.10	3.00	
			$\overline{C_{IN}}$→Fn	1.00	2.10	3.25	
Transition Time	t_{TLH}, t_{THL}	All input		0.50	1.30	2.20	ns

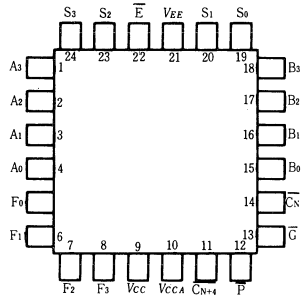
Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

4-bit Binary/BCD ALU

The HD100181F performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (Sn) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable ($\overline{E}$) input open makes the latches transparent.

The circuit uses internal lookahead carry to minimize delay to the F outputs and to the ripple Carry Output, $\overline{Cn+4}$. Group carry lookahead Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are also provided, which are independent of the carry In $\overline{Co}$. The $\overline{P}$ output goes low when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, $\overline{G}$ goes low, when the sum of A and B is greater than fifteen (nine for BCD) in plus mode, or when their difference is greater than zero in a minus mode.

■ PIN ARRANGEMENT

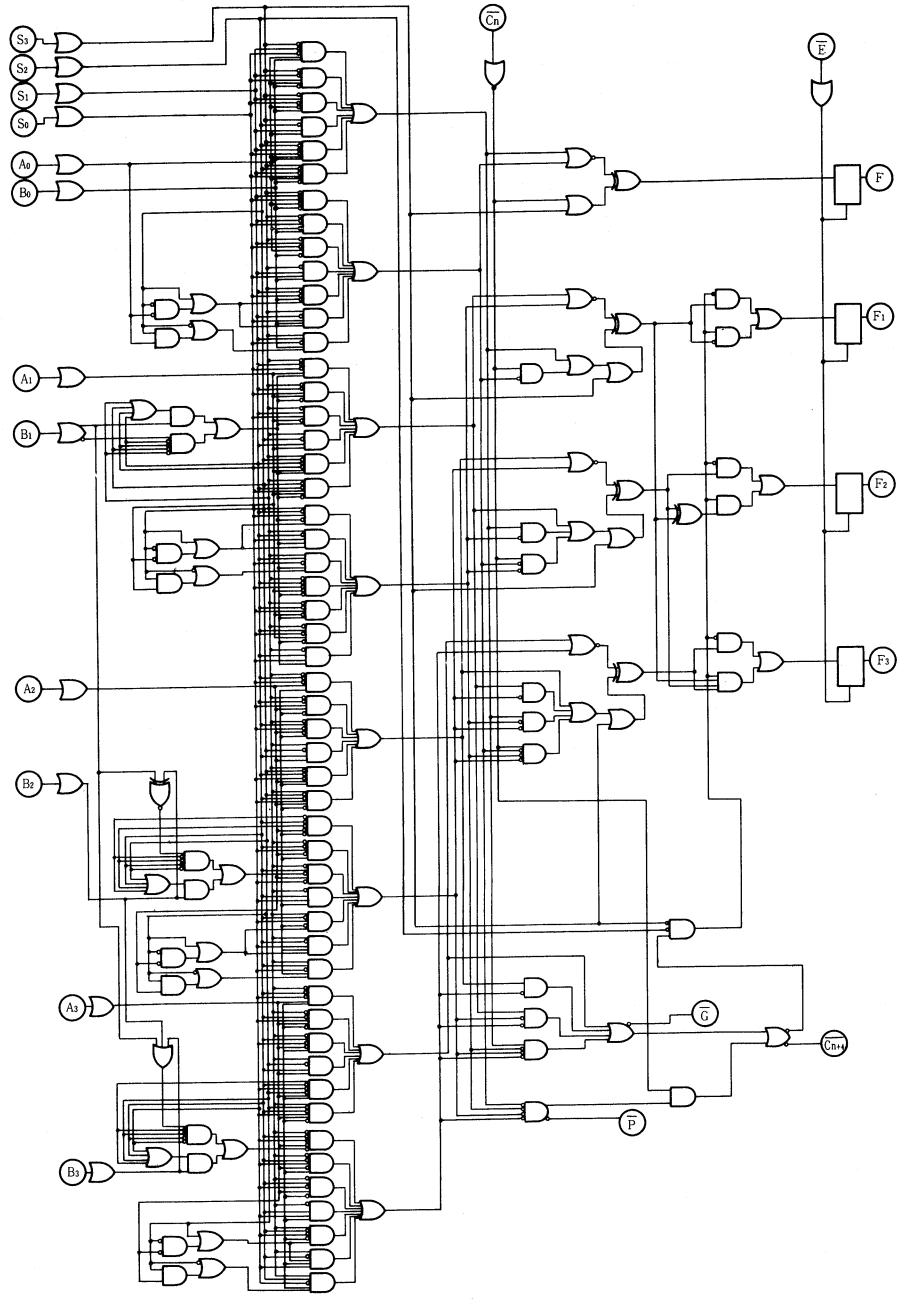


(Top View)

■ FUNCTION SELECT TABLE

S_3	S_2	S_1	S_0	Function
L	L	L	L	A plus B BCD
L	L	L	H	A minus B BCD
L	L	H	L	B minus A BCD
L	L	H	H	0 minus B BCD
L	H	L	L	A plus B Binary
L	H	L	H	A minus B Binary
L	H	H	L	B minus A Binary
L	H	H	H	0 minus B Binary
H	L	L	L	$Fn=AnBn+\overline{An}\overline{Bn}$
H	L	L	H	$Fn=An\overline{Bn}+\overline{An}Bn$
H	L	H	L	$Fn=An+Bn$
H	L	H	H	$Fn=An$
H	H	L	L	$Fn=\overline{Bn}$
H	H	L	H	$Fn=Bn$
H	H	H	L	$Fn=AnBn$
H	H	H	H	$Fn=Low$

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.5V, V_{CC} = GND, Ta = 0 ~ +85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			135	195	270	mA
Input Current	I_{IH}	$V_{IN}=V_{IH}$ max	Sn, $\overline{E}$ input		—	—	350	μA
			Other inputs		—	—	250	
	I_{IL}	$V_{IN}=V_{IL}$ min			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ max or $V_{IN}=V_{IL}$ min		R_T=50Ω	−1025	−955	−880	mV
	V_{OL}			V_{TT}=−2.0V	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH}$ min or $V_{IN}=V_{IL}$ max		R_T=50Ω	−1035	—	—	mV
	V_{OLC}			V_{TT}=−2.0V	—	—	−1610	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■ AC CHARACTERISTICS (V_{EE} = −2.5V, V_{CC} = 2.0V, Ta = 25°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveforms	$\overline{C_0}$→Fn	1.60	3.00	4.40	ns
			$\overline{C_0}$→$\overline{Cn_{+4}}$	1.50	2.45	3.40	
			An, Bn→$\overline{P}$, $\overline{G}$	1.40	2.80	4.20	
			Sn→$\overline{P}$, $\overline{G}$	2.00	3.50	5.00	
			An, Bn→$\overline{Cn_{+4}}$	2.00	3.85	5.70	
			Sn→$\overline{Cn_{+4}}$	2.80	4.80	6.75	
			An, Bn→Fn	2.10	4.00	6.00	
			Sn→Fn	1.50	4.30	7.00	
			$\overline{E}$→Fn	1.30	2.00	2.80	
Transition Time	t_{TLH}, t_{THL}			0.50	1.00	3.50	ns
Setup Time	t_{su}		An, Bn→$\overline{E}$	3.85	—	—	ns
			Sn→$\overline{E}$	4.95	—	—	
			$\overline{Cn}$→$\overline{E}$	2.15	—	—	
Hold Time	t_h		An, Bn→$\overline{E}$	0.20	—	—	ns
			Sn→$\overline{E}$	0.95	—	—	
			$\overline{Cn}$→$\overline{E}$	0.80	—	—	

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5 m/s (500 linear fpm) is maintained.

HITACHI

MÜNCHEN
Hitachi Electronic Components
Europe GmbH
Hans-Pinsel-Straße 3
8013 Haar/b. München
☎ (089) 46 14-0
Telex: 5-22593
Telefax: (089) 46 31 51

DÜSSELDORF
Hitachi Electronic Components
Europe GmbH
Königsallee 6
4000 Düsseldorf
☎ (0211) 8 49 95
Telex: 8-584536
Telefax: (0211) 32 46 12

STUTTGART
Hitachi Electronic Components
Europe GmbH
Fabrikstraße 17
7024 Filderstadt
☎ (0711) 77 20 11
Telex: 7-255267

PARIS
Hitachi Electronic Components
Europe GmbH
Bureau de Représentation en France
95-101, Rue Charles-Michels
F-93200 Saint Denis
☎ 01-8216015
Télex: 611387
Téléfax: 01-2436997

MILANO
Hitachi Electronic Components
Europe GmbH
Via B. Davanzati, 27
I-20158 Milano
☎ 02-3 76 31 44
Telex: 320343
Telefax: 02-683730

LONDON
Hitachi Electronic Components
(UK) Ltd.
Hitec House, 221-225 Station-Road
Harrow, Middlesex, HA1 2XL
☎ 01-8 61 14 14
Telex: 9 36 293
Telefax: 01-8636646

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